

NSWAA/NTWAA

Liverpool 10G

Sunderland 10G

LA-5322P REV 1.0 Schematic

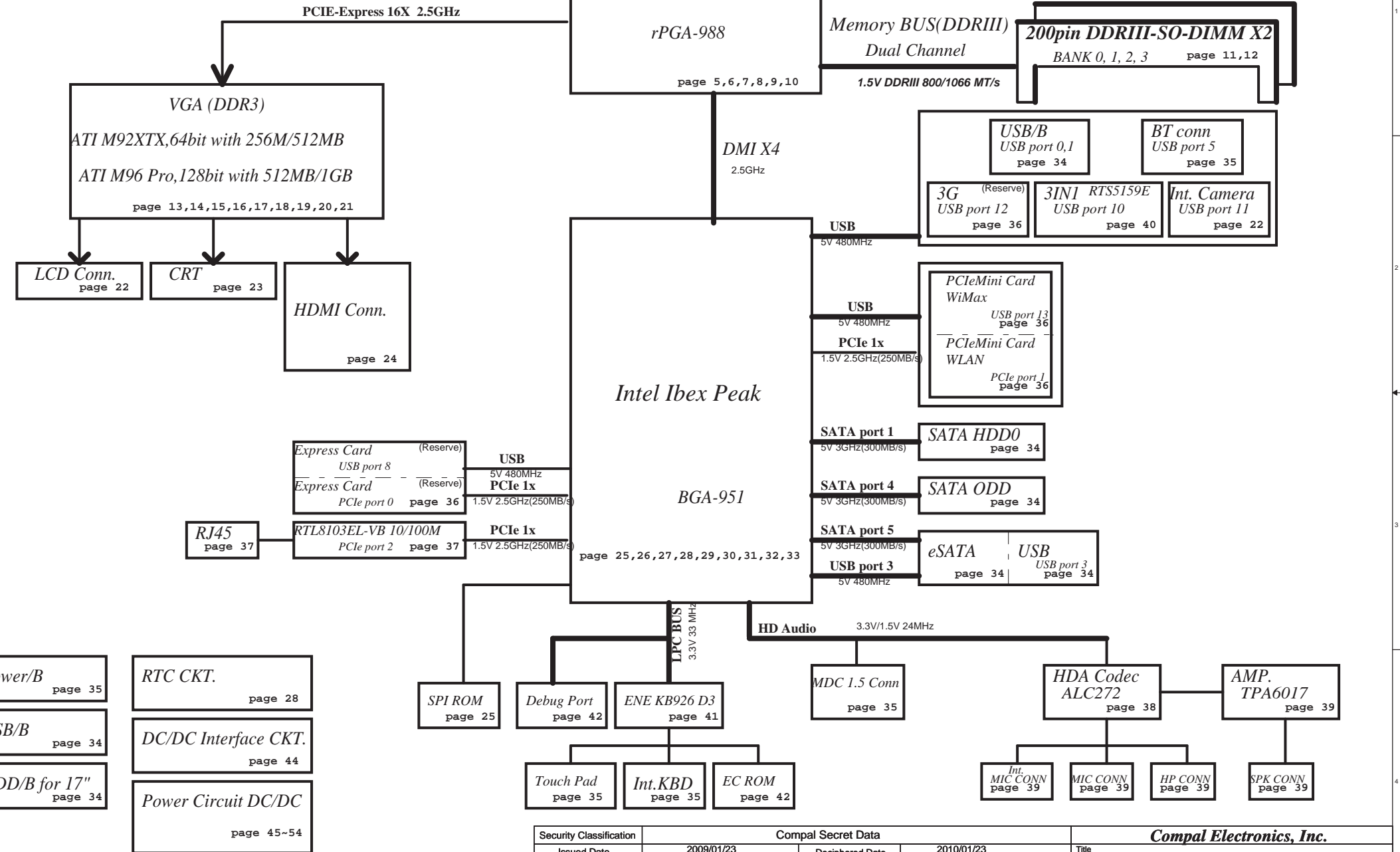
Intel Arrandale /IBEX PEAK
2009-12-22 Rev 1.0

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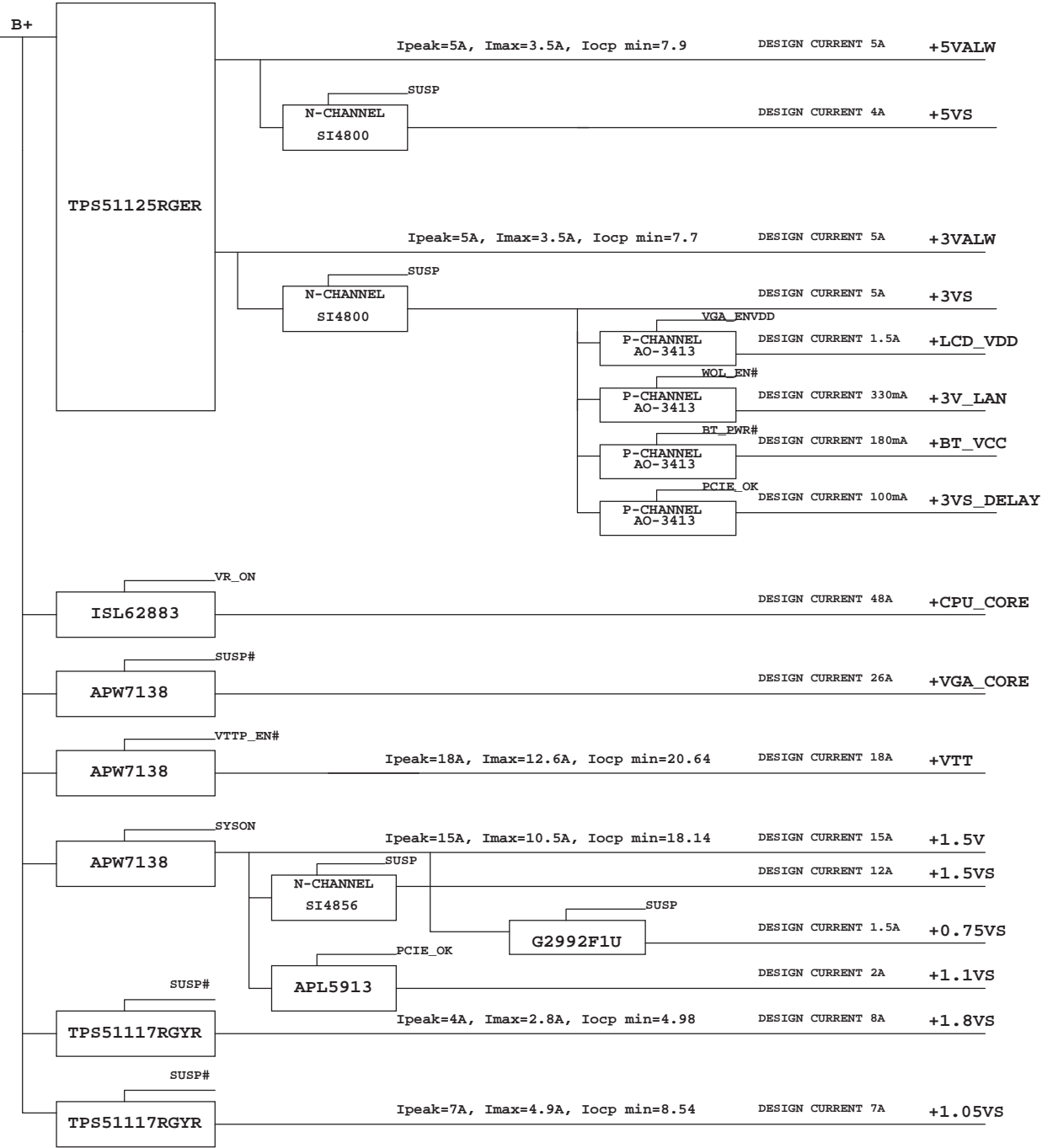
Model Name : NSWAA/NTWAA

File Name : LA-5322P



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NSWAA Liverpool Intel Arrandale (Discrete)
NTWAA Sunderland Intel Arrandale (Discrete)



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Voltage Rails (O MEANS ON X MEANS OFF)

<div>power plane</div> <div>State</div>	+RTCVCC	+B	+5VALW +3VALW +VSB	+1.5V	+5VS +3VS +1.5VS +VGA_CORE +CPU_CORE +VTT +1.05VS +1.8VS +1.1VS +0.75VS
S0	O	O	O	O	O
S1	O	O	O	O	O
S3	O	O	O	O	X
S5 S4/AC	O	O	O	X	X
S5 S4/ Battery only	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X

BTO Option Table

Function	Bluetooth	RJ11	Express Card	MIC	HDMI	Panel		M1/M3	
description	(B)		(E)		(Y)				
explain	Bluetooth	MDC	New Card	MIC	HDMI	16"	17"	M1	M3
BTO	BT@	MDC@	NEW@	MIC@	HDMI@	16@	17@	M1@	M3@

Function	Mini Card	VRAM			GPU	
description						
explain	WIRELESS	256M	512M	1G	M92 XTX	M96 Pro
BTO	WLAN@	2PCS@	4PCS@	8PCS@	M92XTX@	M96PRO@

STATE	SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#
Full ON		HIGH	HIGH	HIGH
S1(Power On Suspend)		HIGH	HIGH	HIGH
S3 (Suspend to RAM)		LOW	HIGH	HIGH
S4 (Suspend to Disk)		LOW	LOW	HIGH
S5 (Soft OFF)		LOW	LOW	LOW
G3		LOW	LOW	LOW

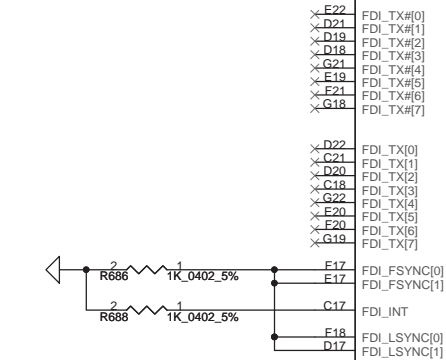
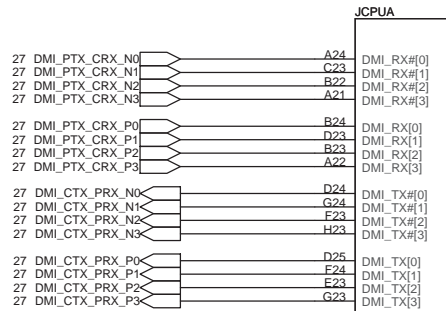
EC SM Bus1 address EC SM Bus2 address

Power	Device	Address	Power	Device	Address
+3VALW	EC KB926 D3		+3VS	EC KB926 D3	
+3VALW	Smart Battery	0001 011x b	+3VS	VGA THM Sensor ADM1032ARMZ	1001 110x b
			+3VS	PCH	0100 110x b

PCH SM Bus address

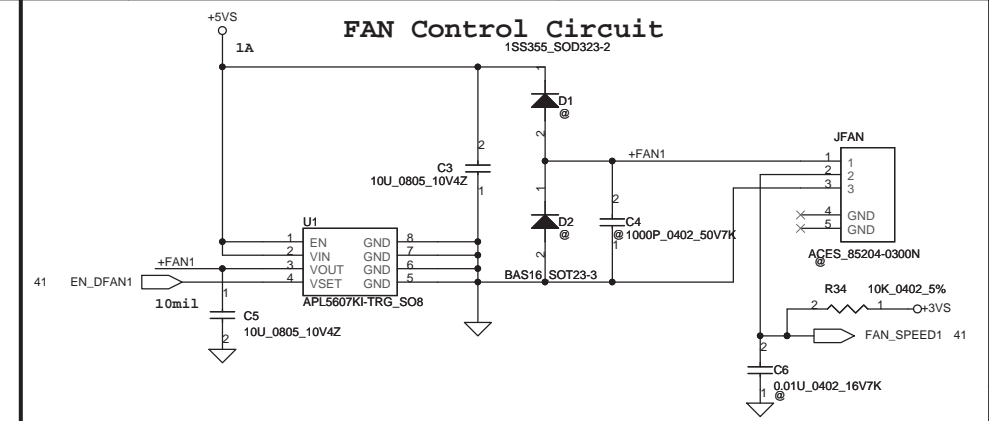
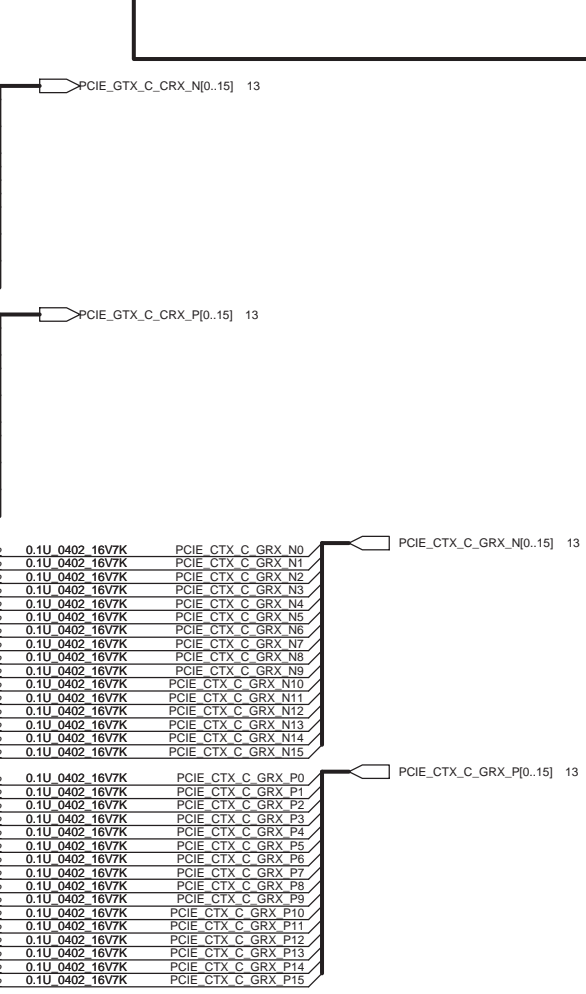
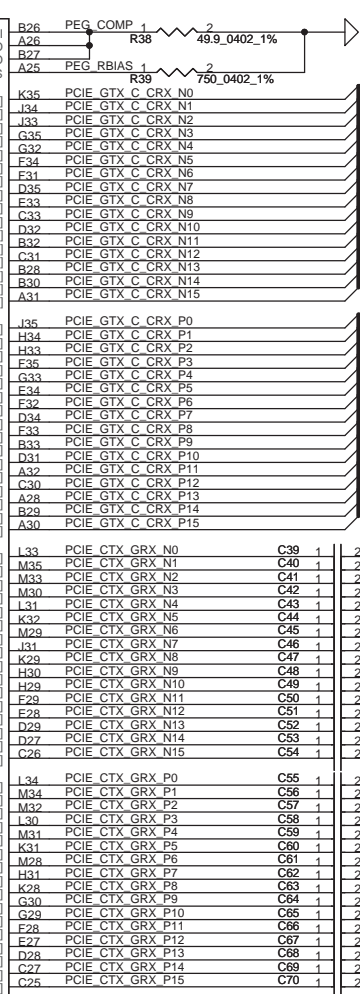
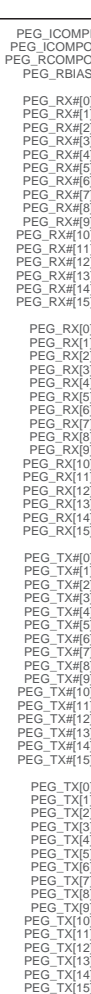
Power	Device	Address
+3VALW	PCH	
+3VS	Clock Generator	1101 001x b
+3VS	DDR DIMM0	1001 000x b
+3VS	DDR DIMM1	1001 010x b
+3VS	Express	
+3VS	WLAN/Wimax/3G	

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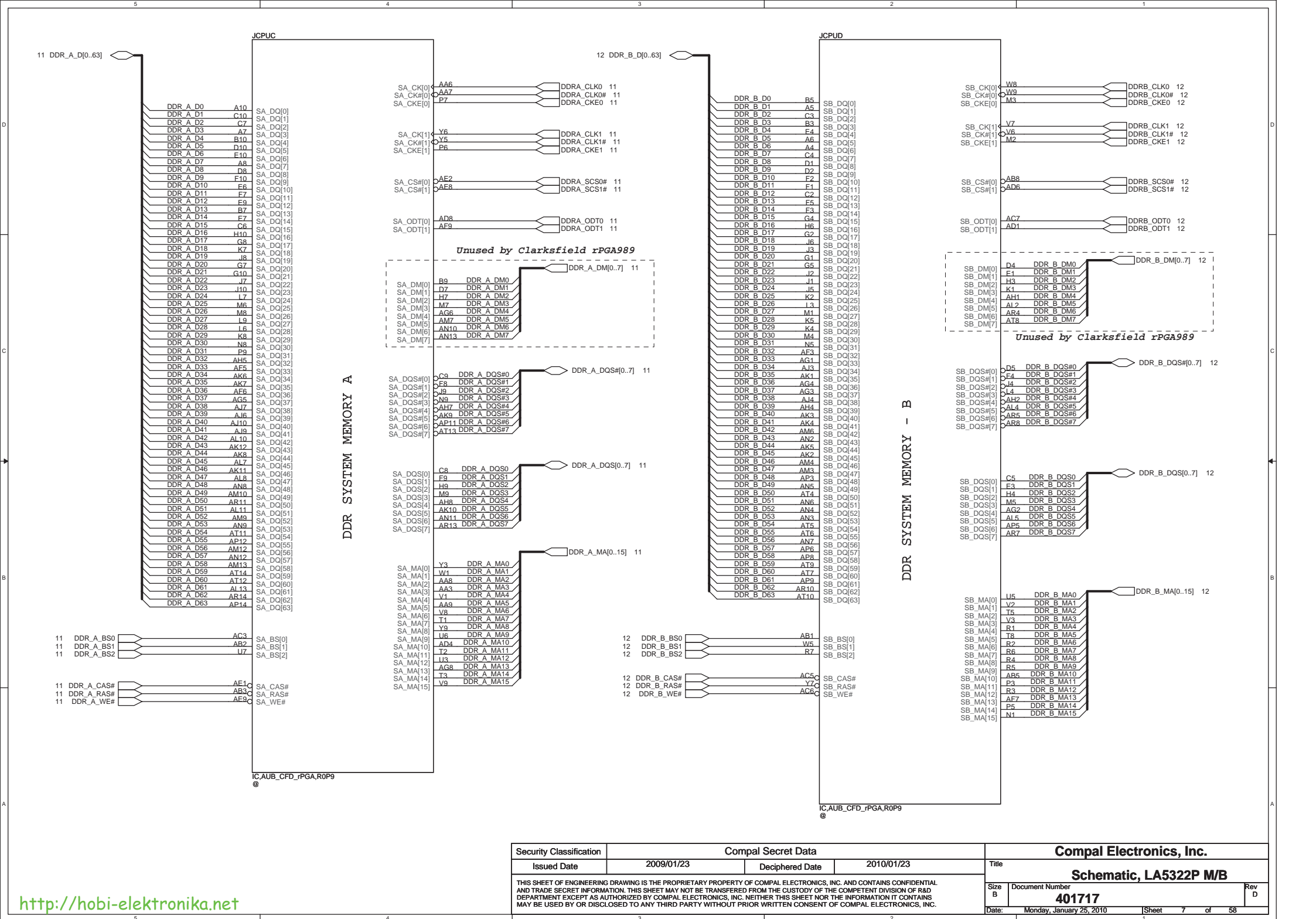
IC_AUB_CFD_rPGA_R0P9

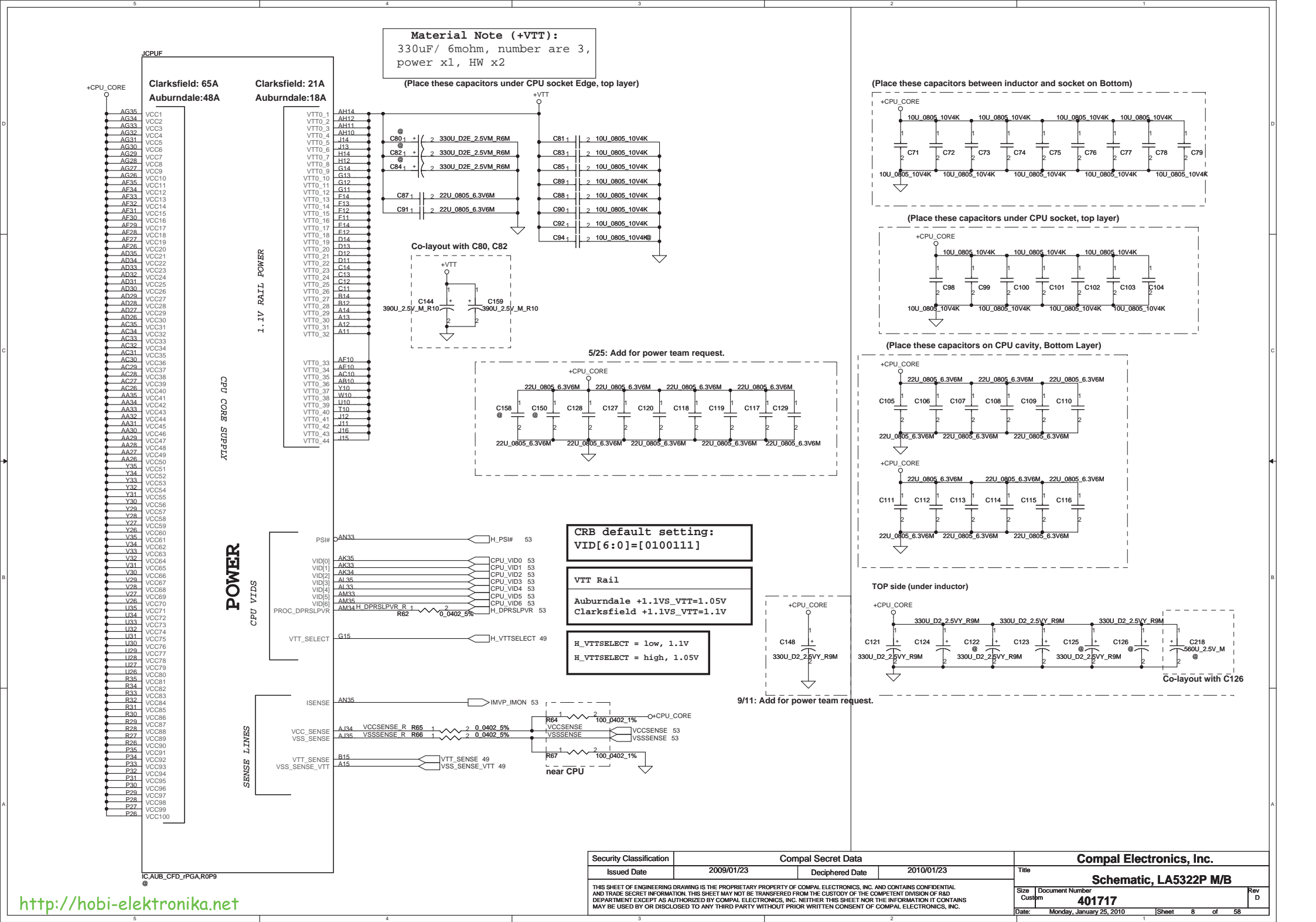
PCI EXPRESS -- GRAPHICS

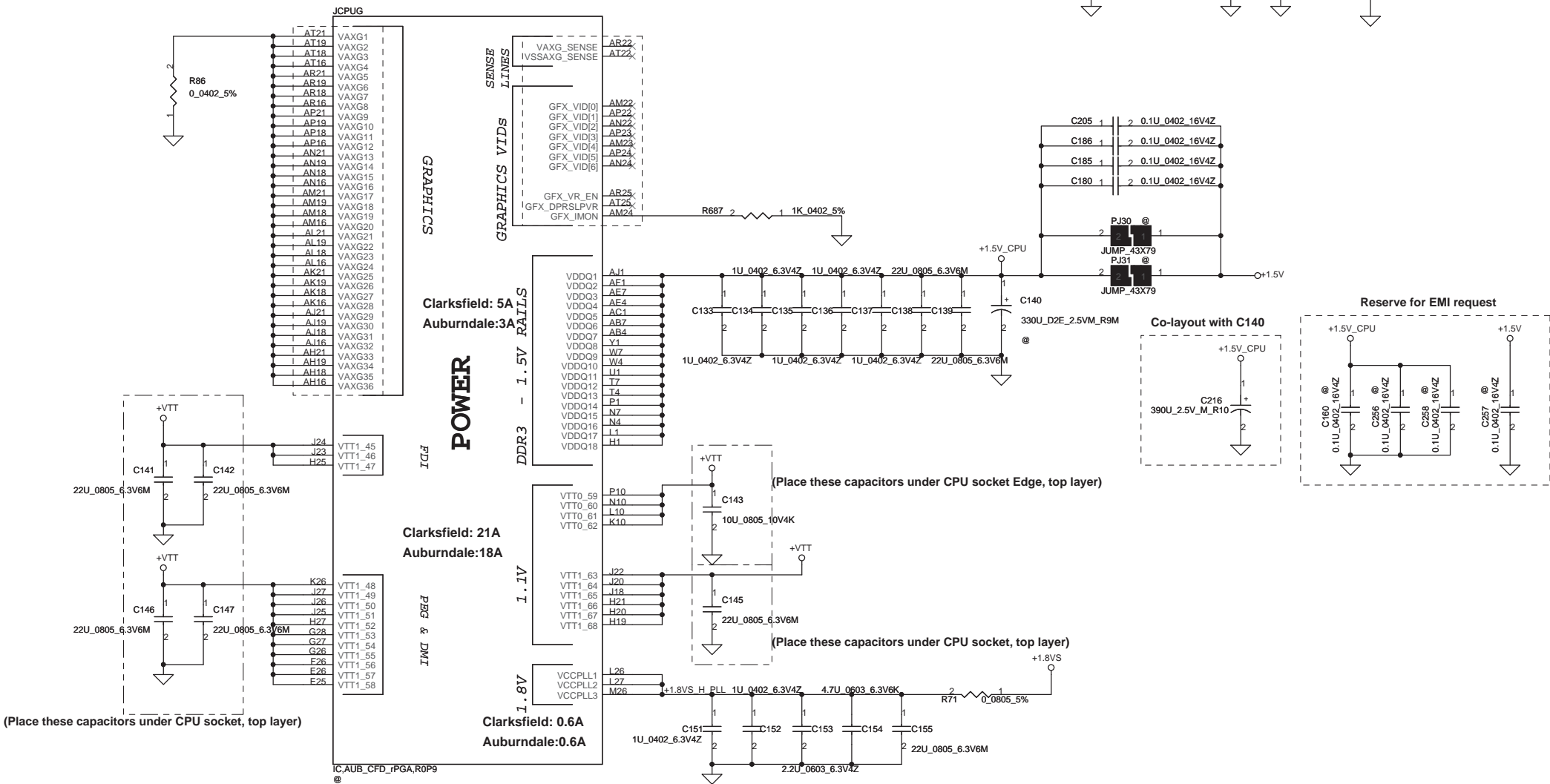


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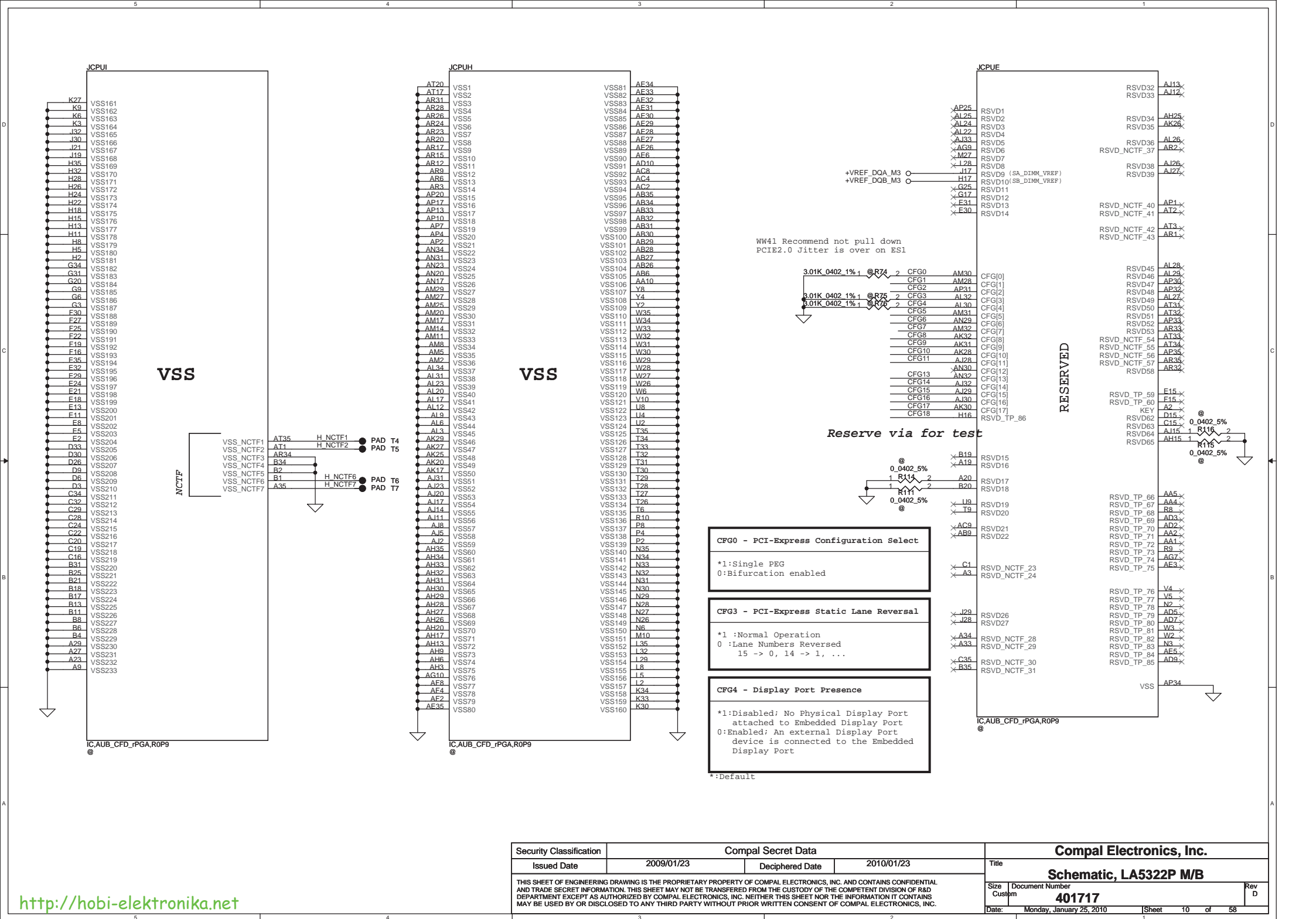
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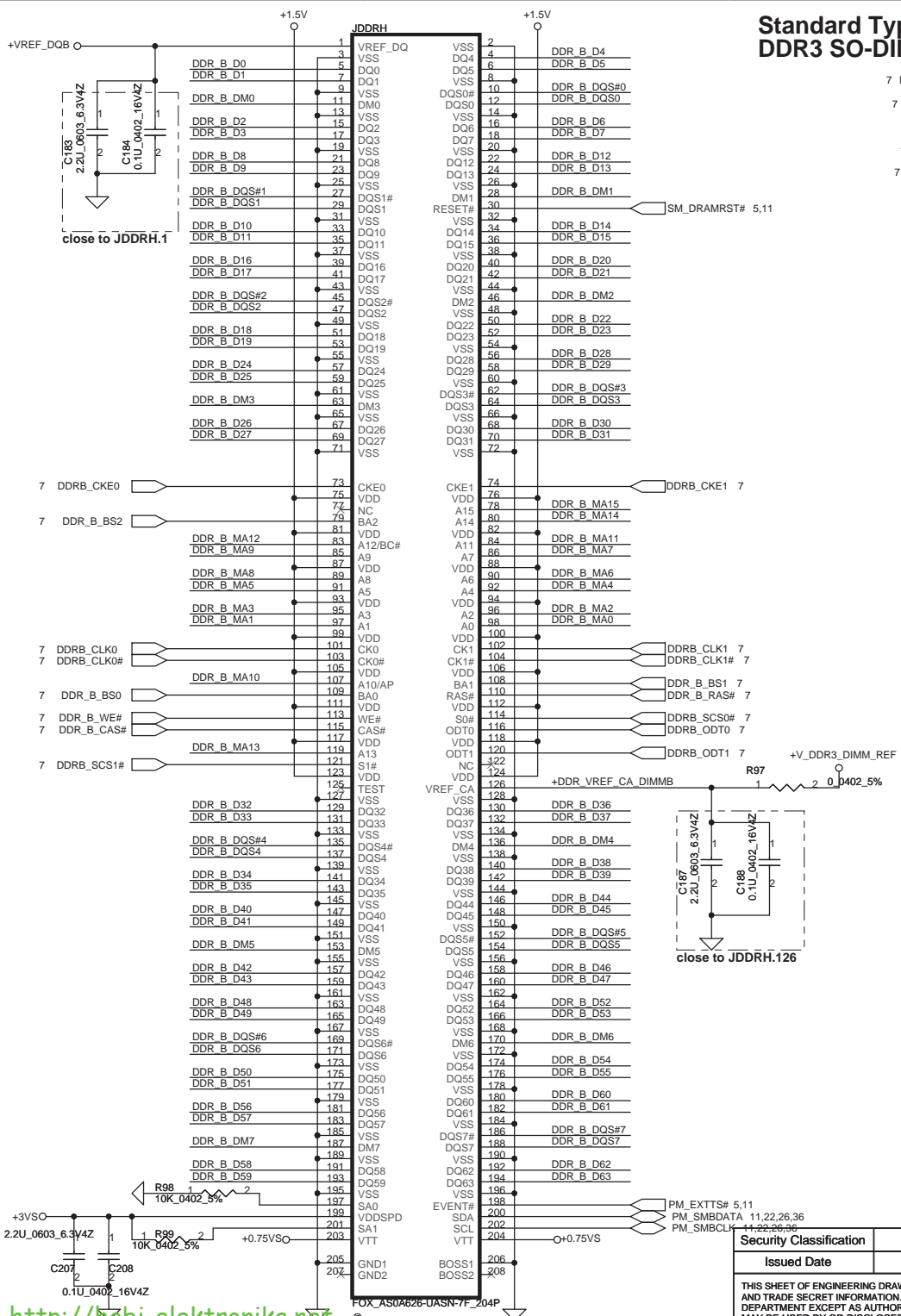


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Standard Type DDR3 SO-DIMM B

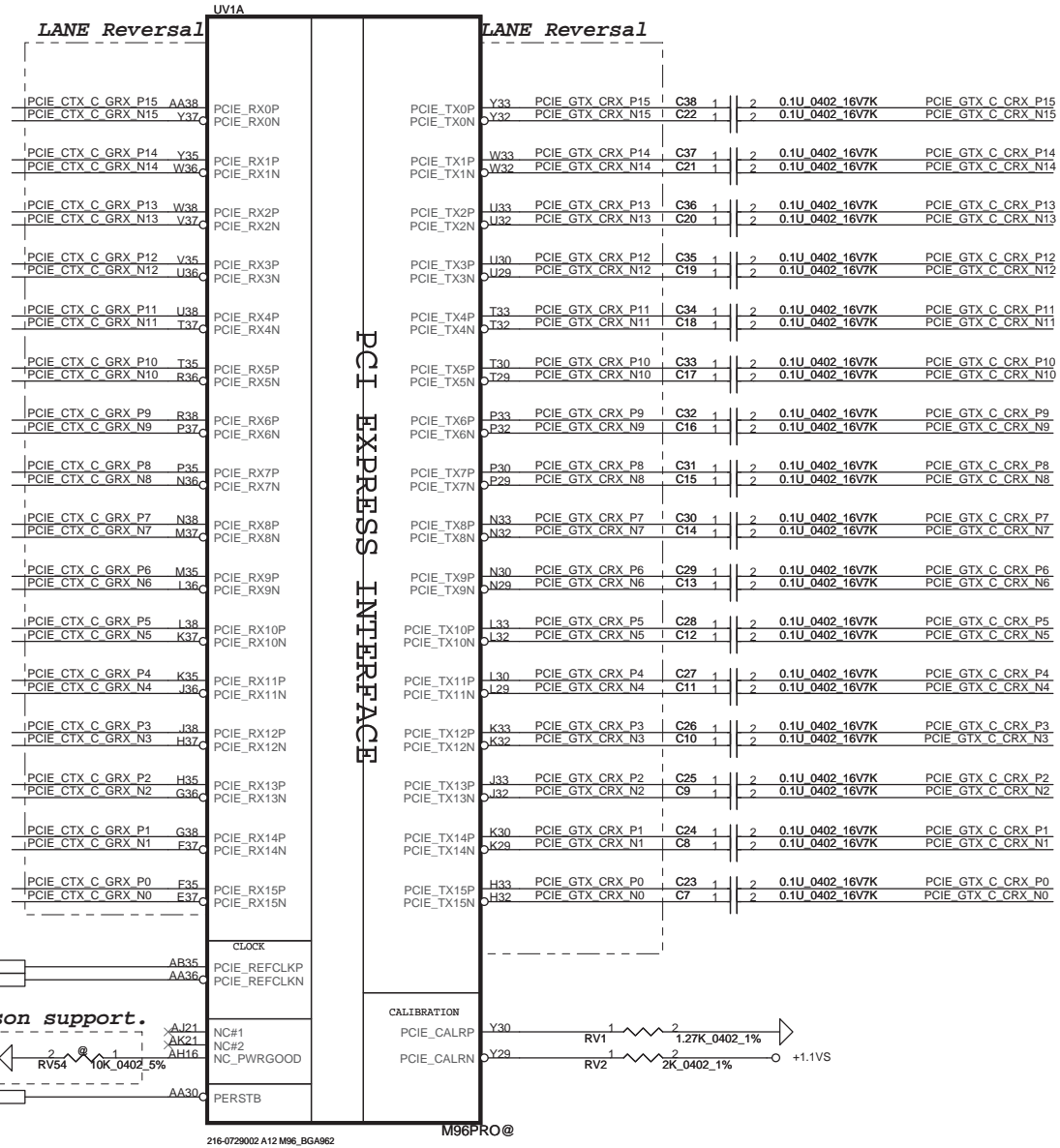
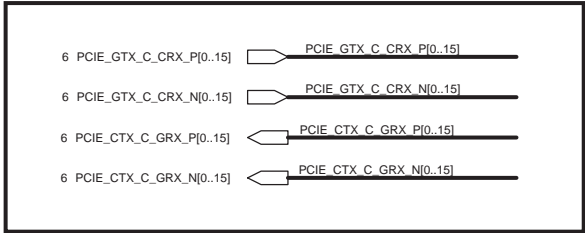
- 7 DDR_B_DQS#[0..7]
- 7 DDR_B_DQS[0..7]
- 7 DDR_B_D[0..63]
- 7 DDR_B_DM[0..7]
- 7 DDR_B_MA[0..15]

Layout Note:
Place near JDDR.H

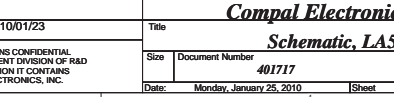
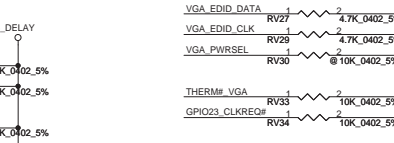
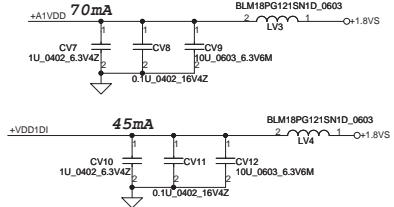
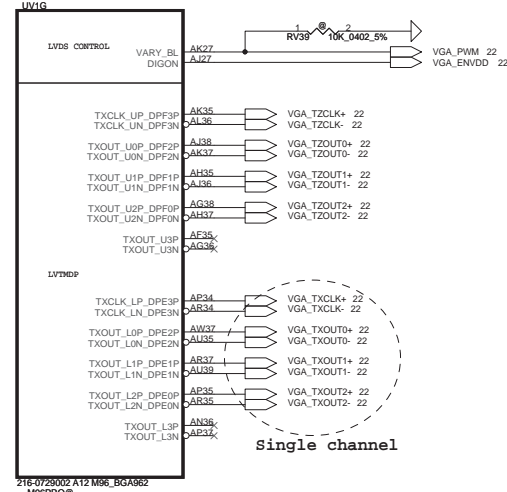
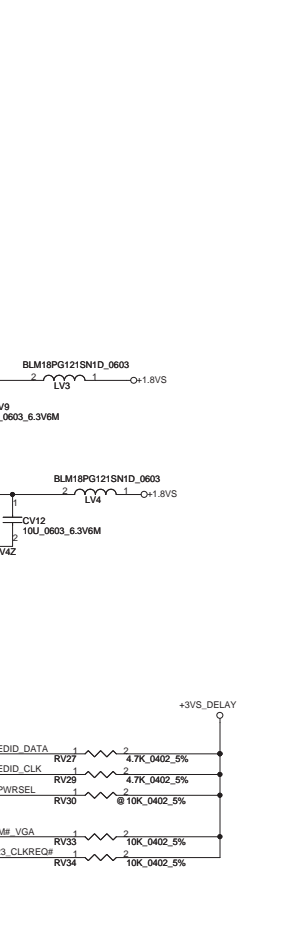
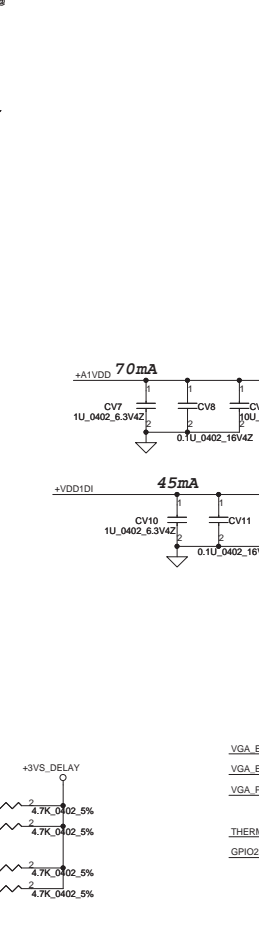
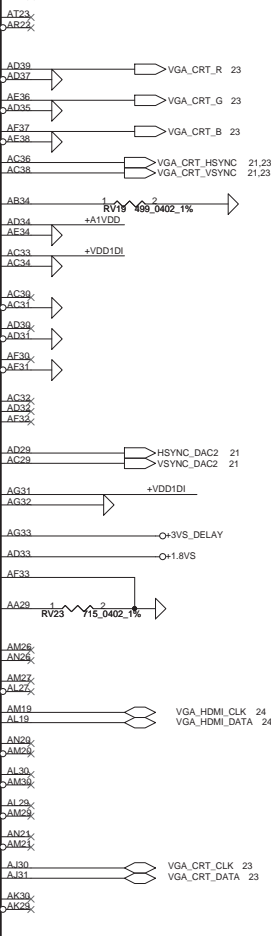
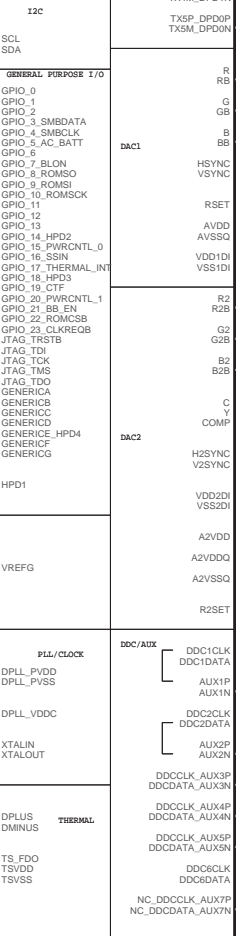
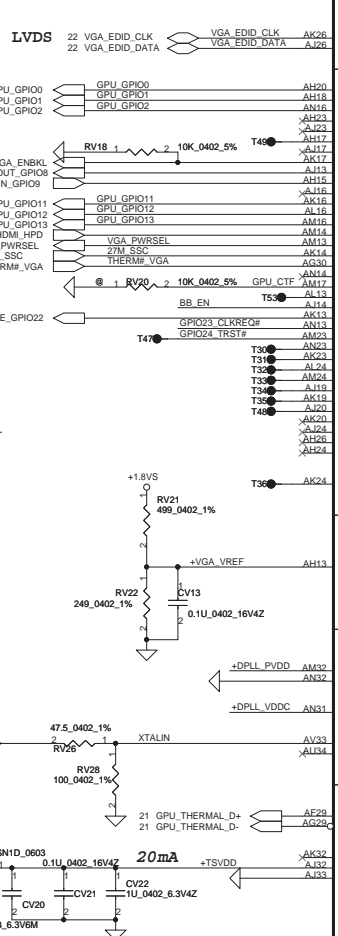
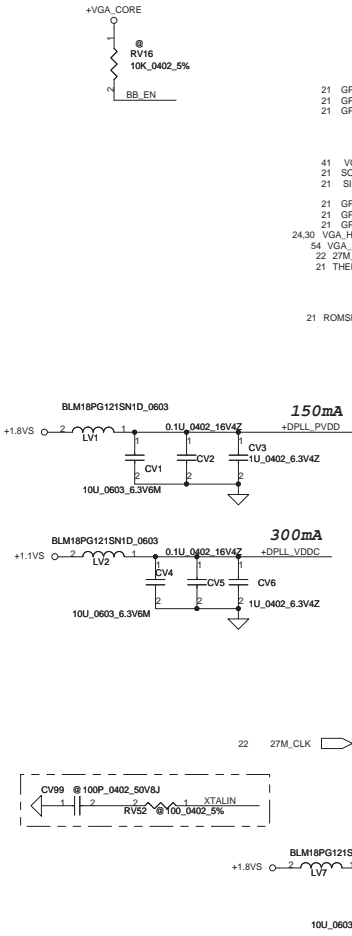
Layout Note: Place these 4 Caps near
Command and Control signals of DIMMB

Layout Note:
Place near JDDR.H.203 and 204

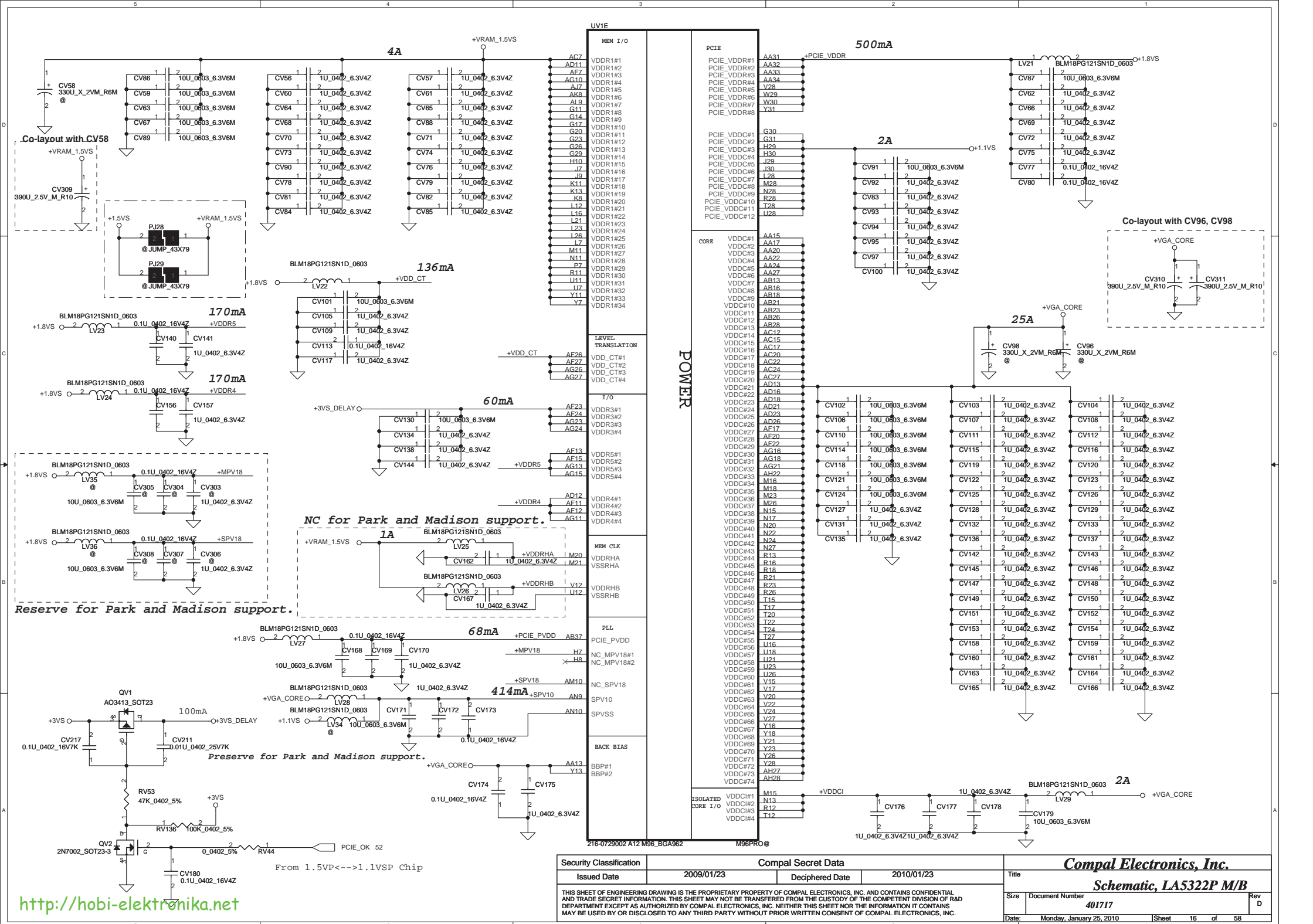
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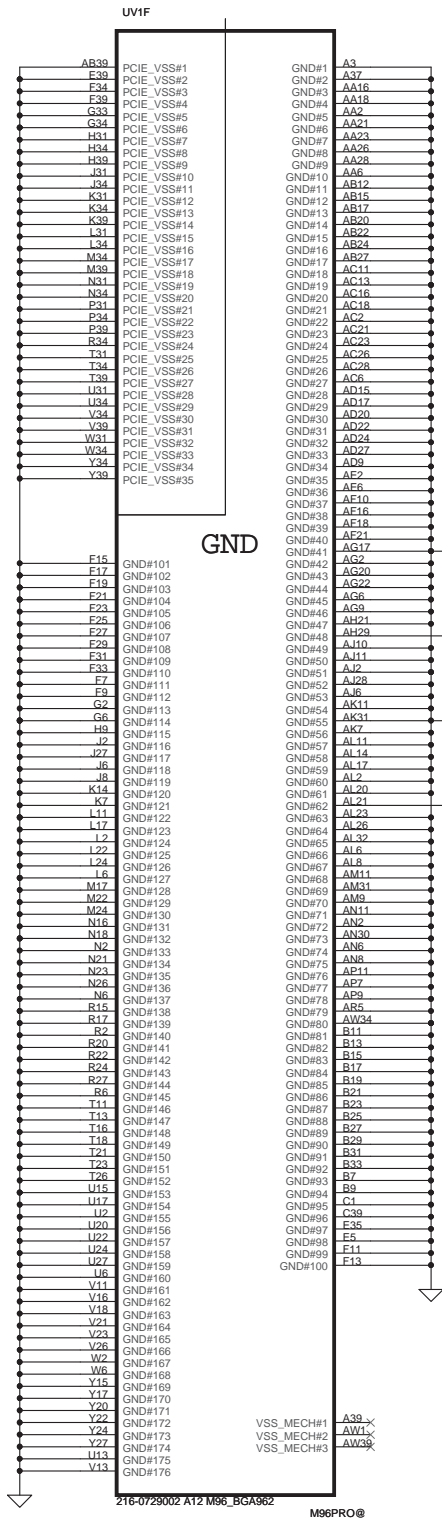


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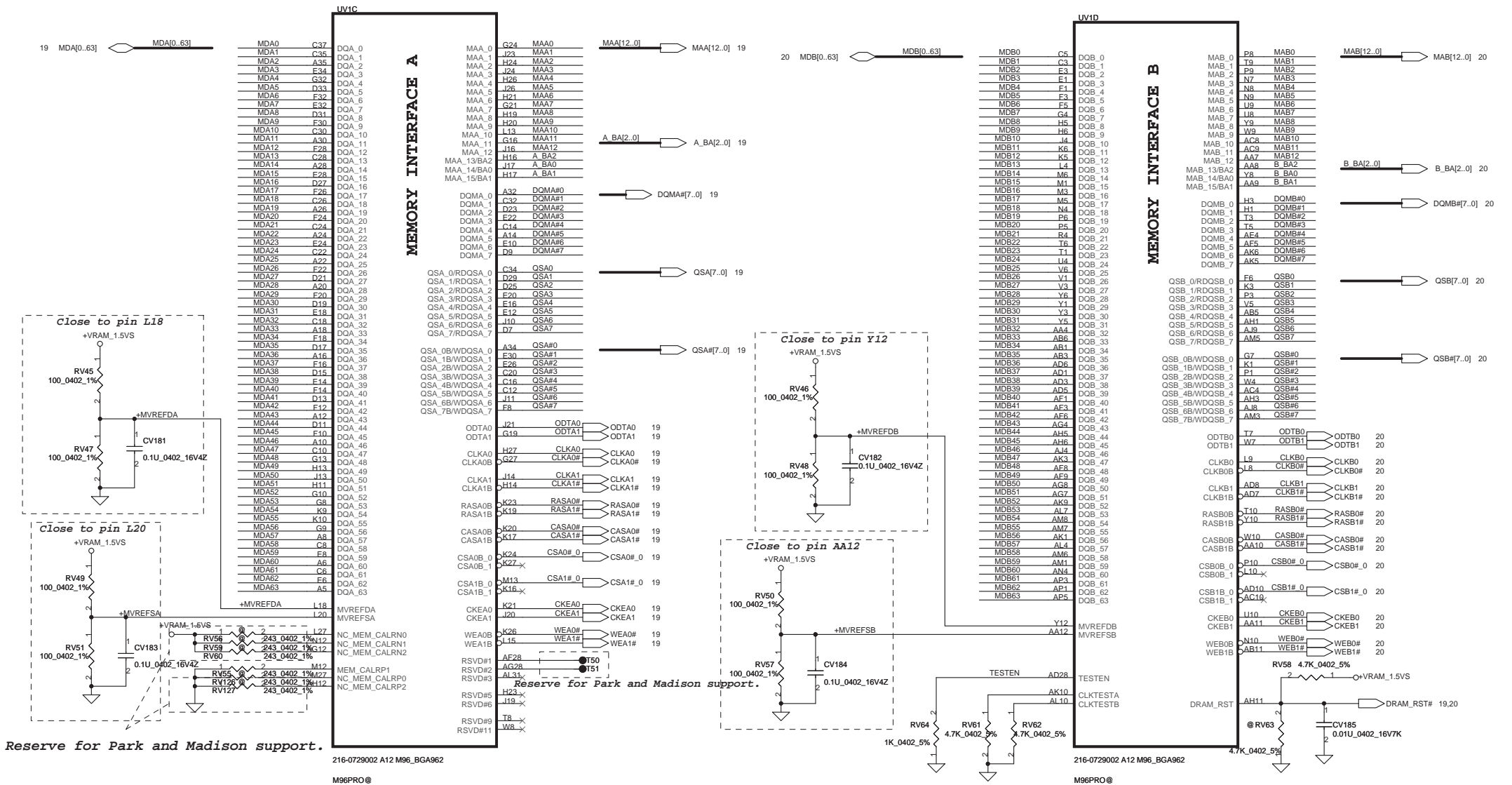
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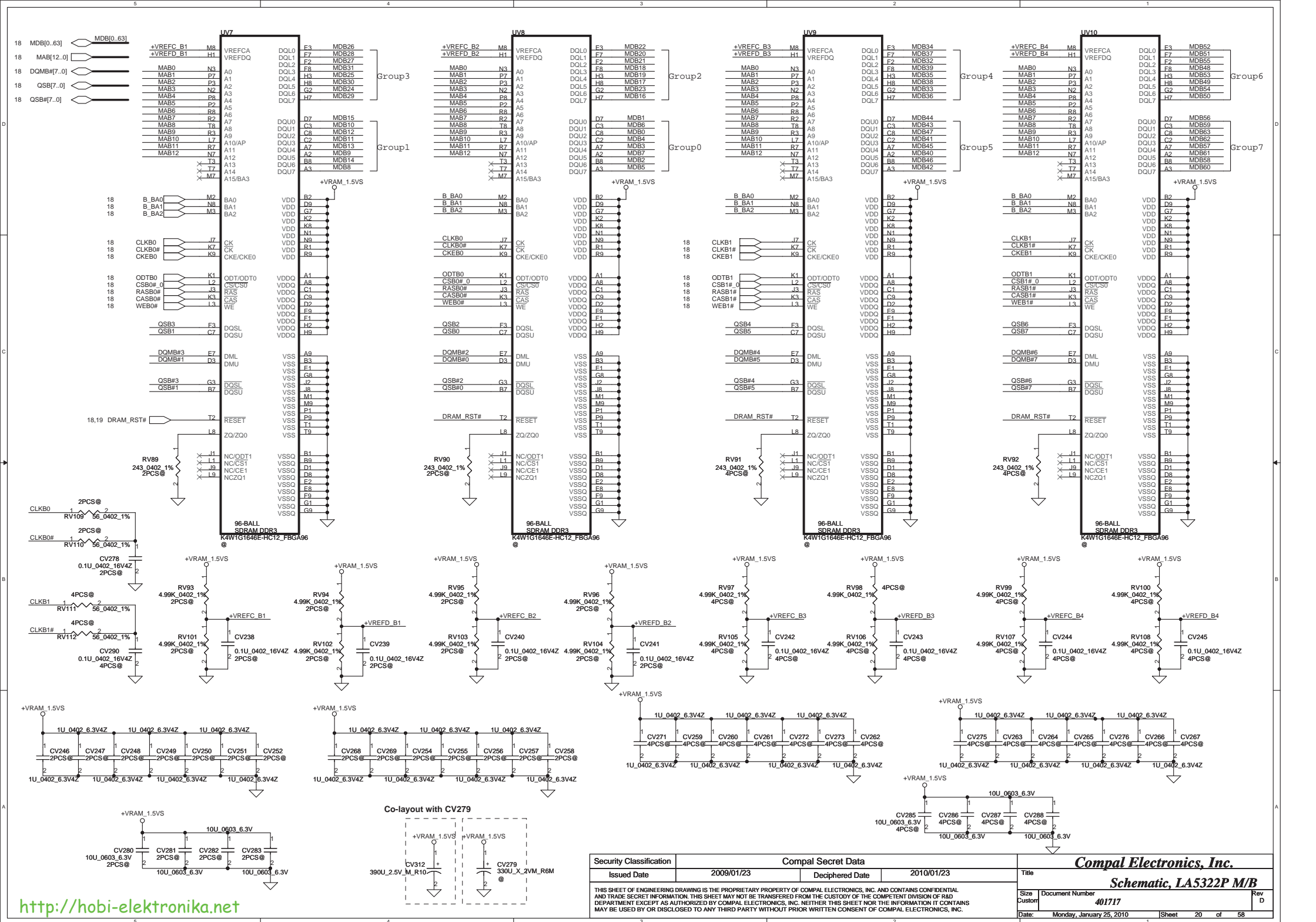
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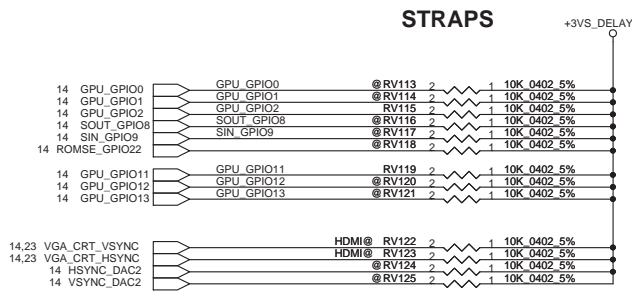


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GPU by the system BIOS		GPU by VBIOS	
GPIO22 = 0 (BIOS_ROM_EN = 0)		GPIO22 = 1 (BIOS_ROM_EN = 1)	
GPIO[13:11]		MEMORY SIZE	GPIO[13:11]
0 0 0		128MB	1 0 0 (M25P05A)
0 0 1		256MB	
0 1 0		64MB	



CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	0
BIF_GEN2_EN_A	GPIO2	PCIE GNE2 ENABLED	1
BIF_CLK_PM_EN	GPIO8	BIF_CLK_PM_EN	0
BIF_VGA_DIS	GPIO9	VGA Controller ENABLED	0 (Enable)
BIOS_ROM_EN	GPIO_22_ROMCSB	Enable External BIOS device	0
ROMIDCFG(2:0)	GPIO[13:11]	ROM Configurations	0 0 1
VIP_DEVICE_STRAP_ENA	VSUNC_DAC2	IGNORE VIP DEVICE STRAPS	0
AUD[1]	HSUNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	1 1
AUD[0]	VSUNC		
RSVD	HSUNC_DAC2		0
RSVD	GENERICC		0

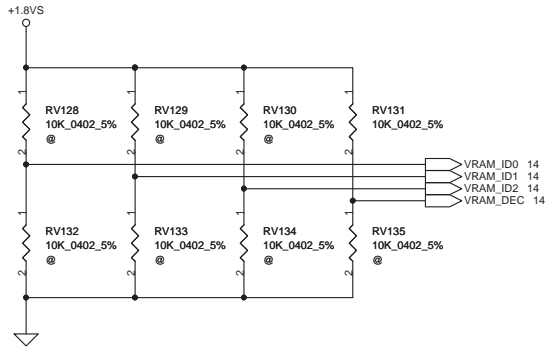
AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

HSUNC_DAC2 GENERICC

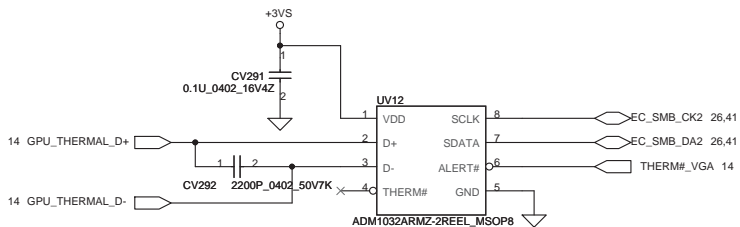
PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

GPIO_28_TDO GPIO21_BB_EN



DDR3	
VRAM_DEC	1

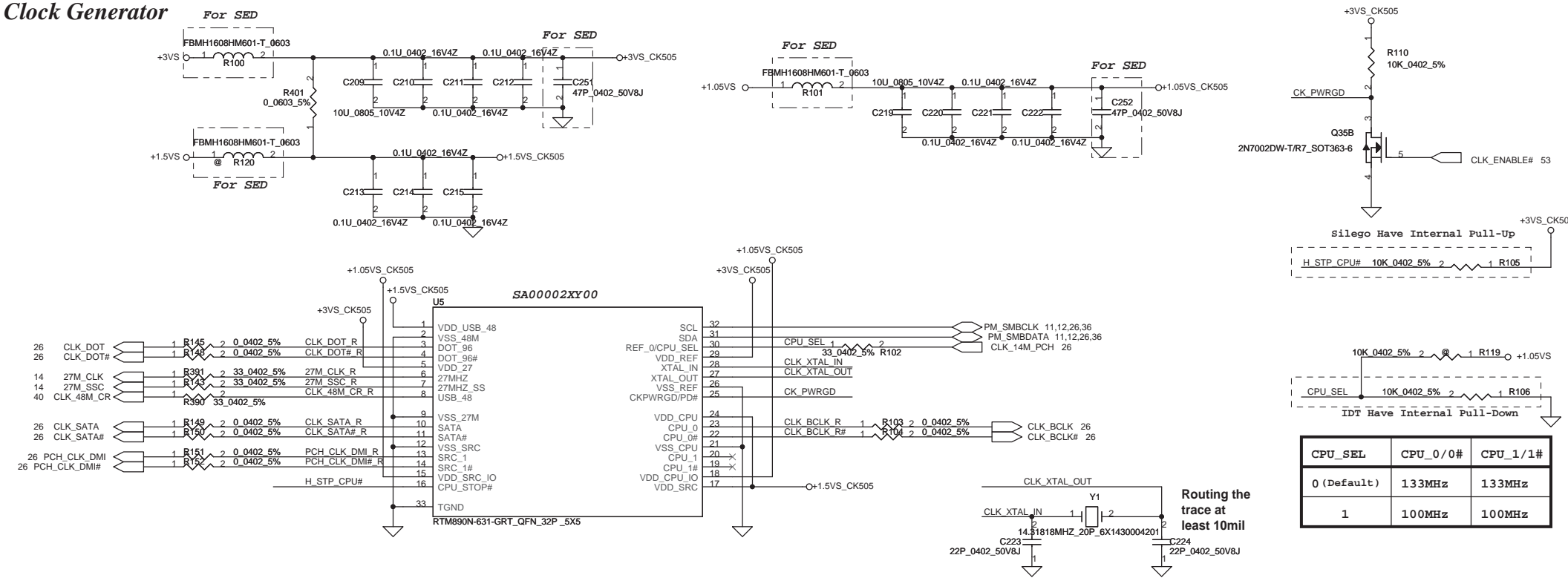
External VGA Thermal Sensor



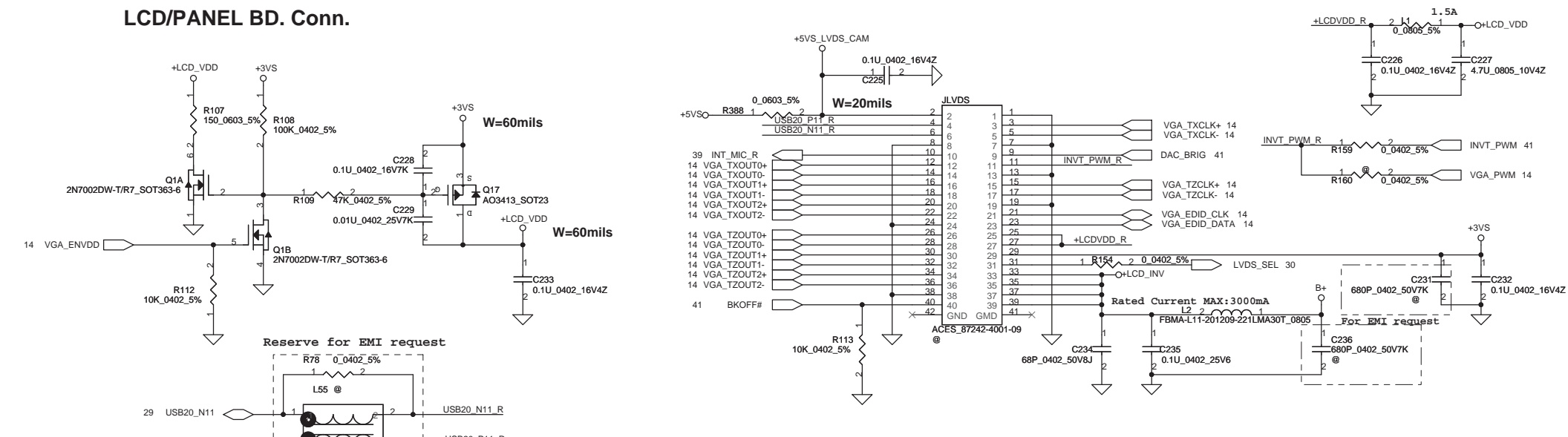
STRAPS	PIN	GPU	VRAM size	Vendor Part Number#	Compal Part Number#	VRAM_ID 2,1,0
VRAM_ID[2:0]	DVPDATA (3,2,1)	M92-M2 XT	512M 64Mx16 (x4)	HYN H5TQ1G63BFR-12C	SA000032400	0 0 0
		M96-M2	1G 64Mx16 (x8)	HYN H5TQ1G63BFR-12C	SA000032400	0 0 1
		M92-M2 XT	256M 64Mx16 (x2)	HYN H5TQ1G63BFR-12C	SA000032400	0 1 0
		M96-M2	1G 64Mx16 (x8)	SAM K4W1G1646E-HC12	SA000035700	0 1 1
		M92-M2 XT	512M 64Mx16 (x4)	SAM K4W1G1646E-HC12	SA000035700	1 0 0
		M92-M2 XT	256M 64Mx16 (x2)	SAM K4W1G1646E-HC12	SA000035700	1 0 1

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Clock Generator

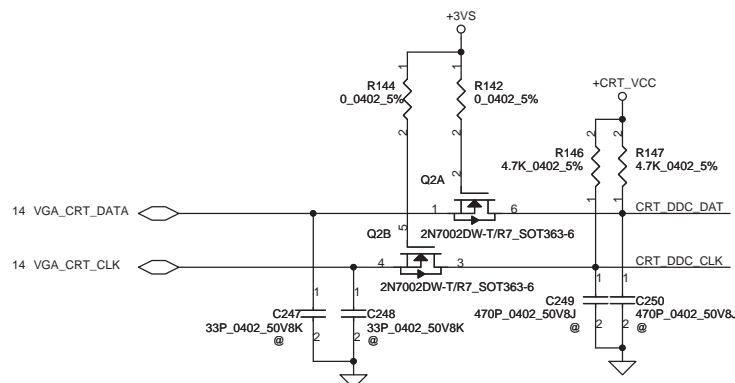
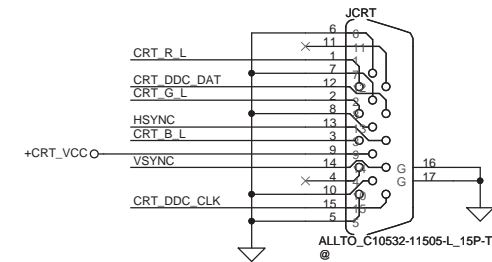
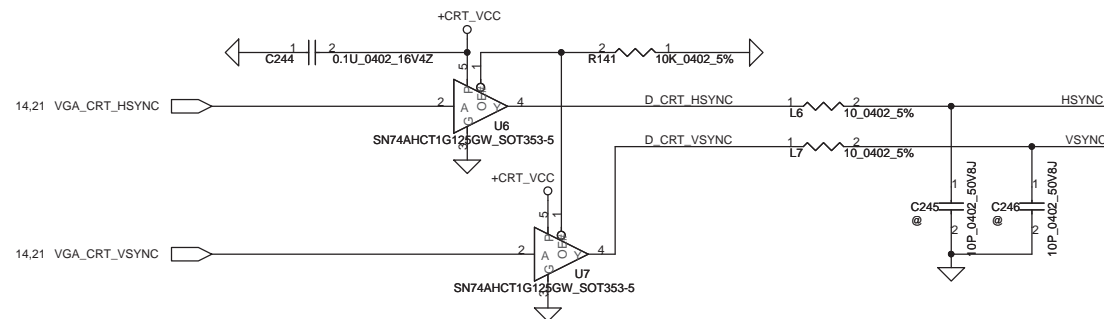
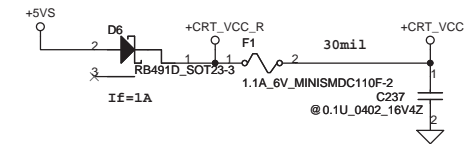
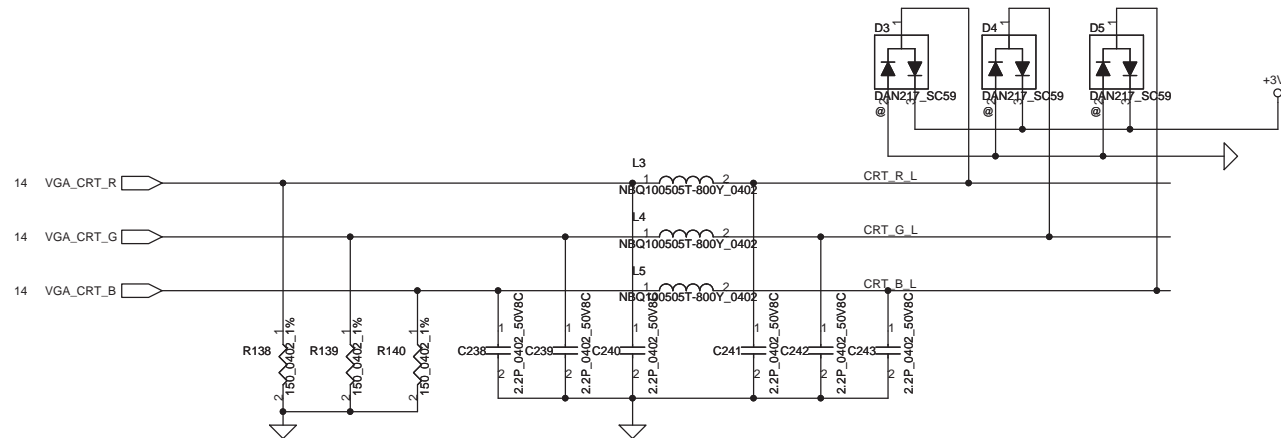


LCD/PANEL BD. Conn.

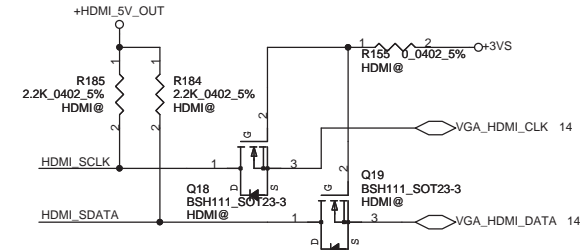
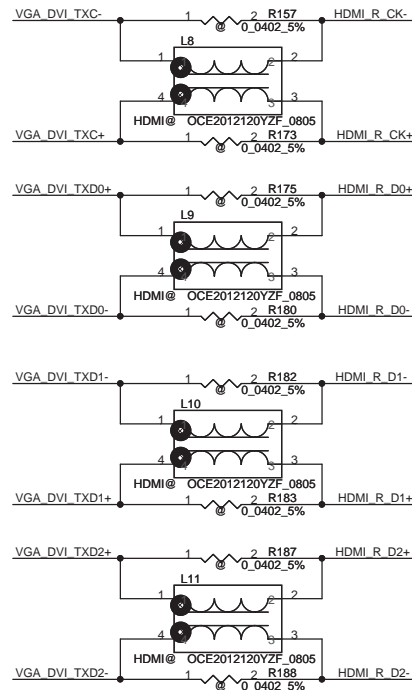
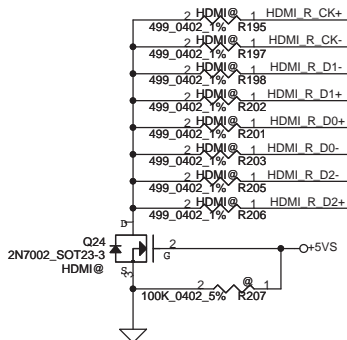
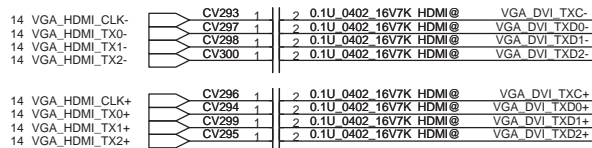
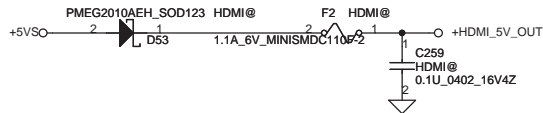


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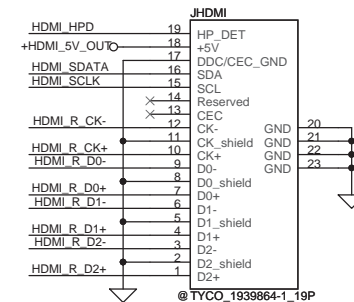
CRT CONNECTOR



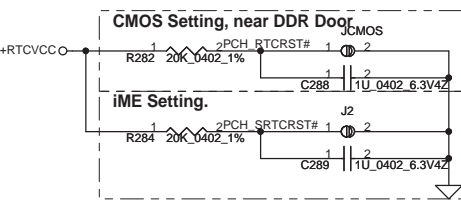
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HDMI Connector



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Integrated SUS 1.05V VRM Enable

PCH_INTVRMEN

High - Enable Internal VRs
(must be always pulled high)

HDA_SYNC

This signal has a weak internal pull down.
H=>On Die PLL is supplied by 1.5V
*L=>On Die PLL is supplied by 1.8V

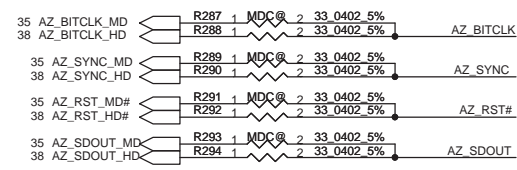
HDA_SDO

This signal has a weak internal pull down.
This signal can't PU

Flash Descriptor Security Override

HDA_DOCK_EN#

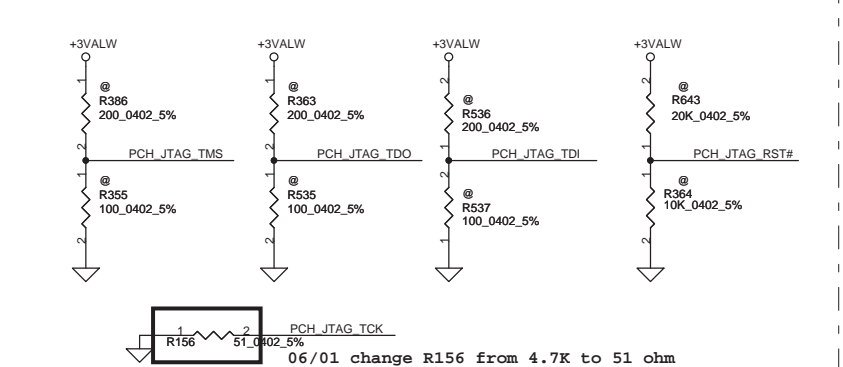
Low = Enabled
High = Disabled *



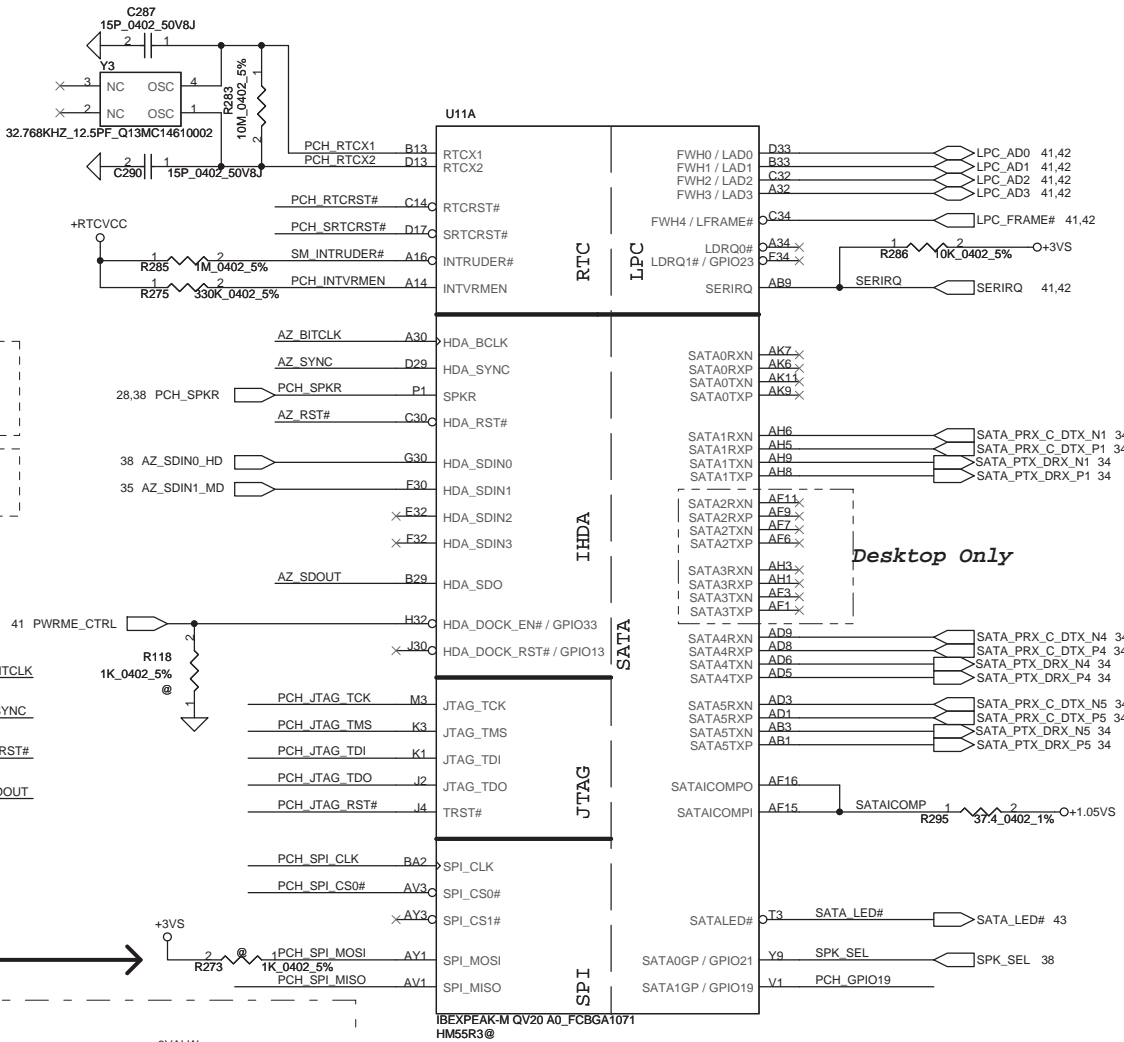
ITPM Enabled Internal: Pull down 20k

SPI_MOSI

High = Enabled
Low = Disabled (Default)



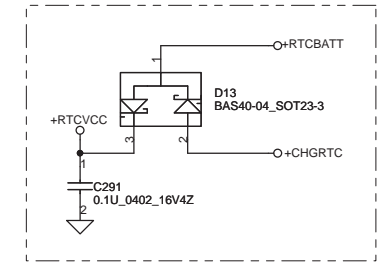
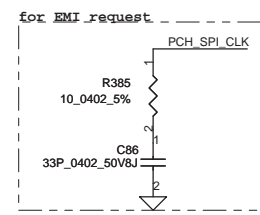
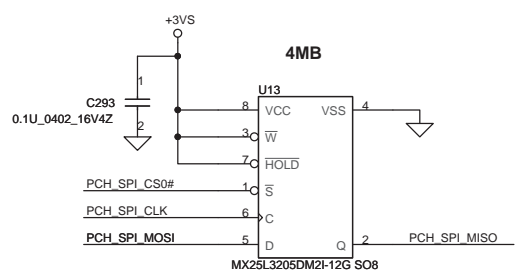
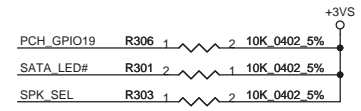
PCH Pin	RefDes	PCH JTAG Enable		PCH JTAG Disable (Default)	
		ES1	ES2	ES1	ES2
PCH_JTAG_TDO	R358	No Install	200ohm	No Install	No Install
R355	No Install	100ohm	No Install	No Install	No Install
PCH_JTAG_TMS	R355	200ohm	200ohm	No Install	No Install
R354	100ohm	100ohm	No Install	No Install	No Install
PCH_JTAG_TDI	R536	200ohm	200ohm	20kohm	No Install
R537	100ohm	100ohm	10kohm	No Install	No Install
PCH_JTAG_TCK	R156	51ohm	51ohm	51ohm	51ohm
R643	20kohm	20kohm	No Install	No Install	No Install
PCH_JTAG_RST#	R643	20kohm	20kohm	No Install	No Install
R537	No Install	No Install	No Install	No Install	No Install



1ST HDD

SATA ODD

eSATA



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For NewCard

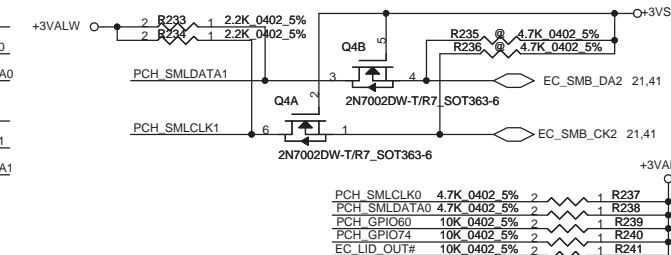
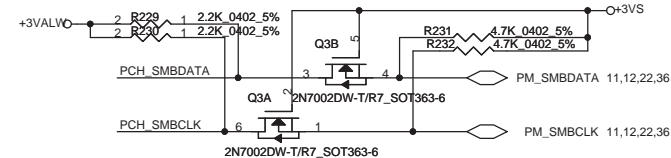
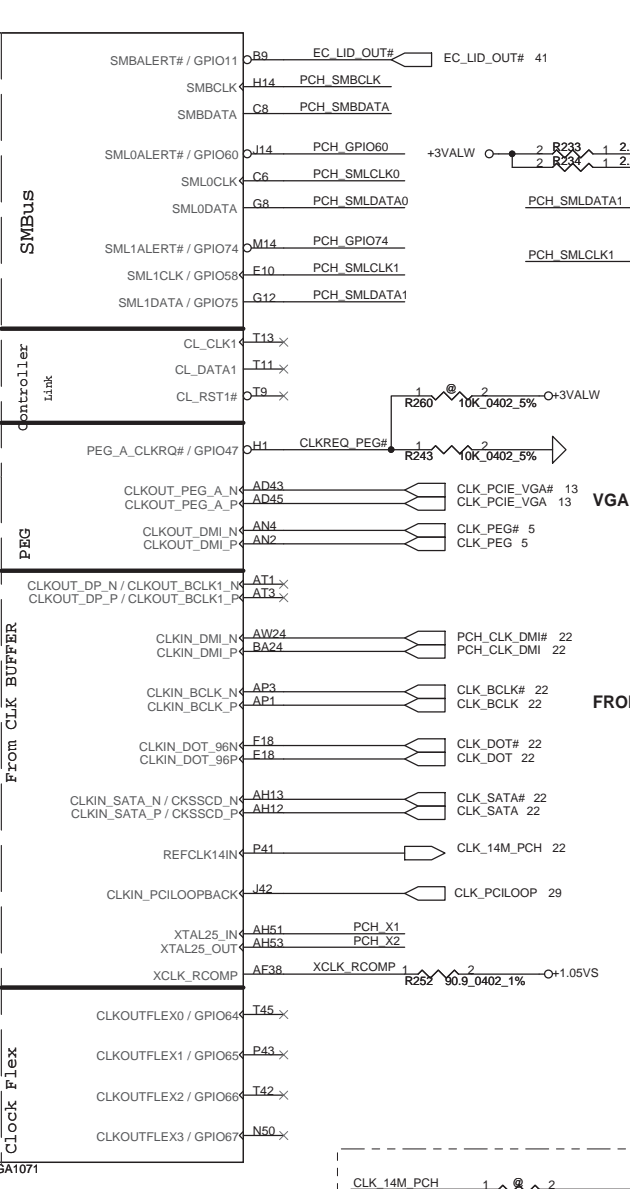
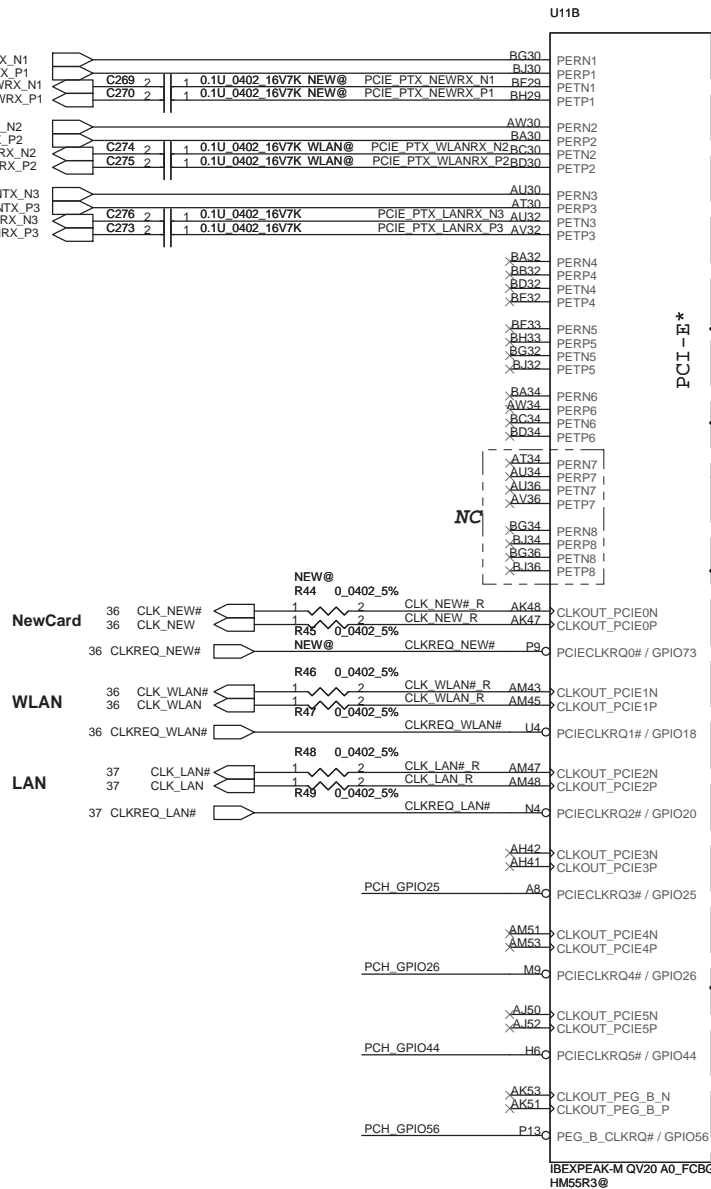
36 PCIE_PRX_NEWTX_N1
36 PCIE_PRX_NEWTX_P1
36 PCIE_PTX_C_NEWRX_N1
36 PCIE_PTX_C_NEWRX_P1

For WLAN

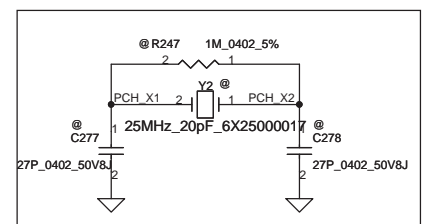
36 PCIE_PRX_WLANTX_N2
36 PCIE_PRX_WLANTX_P2
36 PCIE_PTX_C_WLANRX_N2
36 PCIE_PTX_C_WLANRX_P2

For LAN

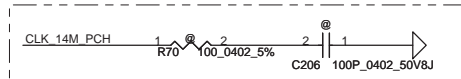
37 PCIE_PRX_C_LANTX_N3
37 PCIE_PRX_C_LANTX_P3
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37 PCIE_PTX_C_LANRX_P3



FROM CLK GEN FOR: 133/100/96/14.318 MHZ

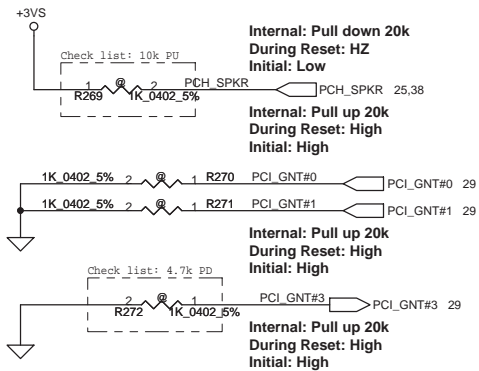


Note: Stuff 0 ohm if 25MHz crystal un-stuff



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PCH Strap Pin



NO REBOOT Strap

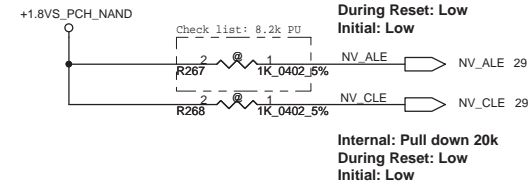
PCH_SPKR	Low= Disable High= Enable
----------	------------------------------

Boot BIOS Strap

PCI_GNT#1	PCI_GNT#0	Boot BIOS Loaction
0	0	LPC (Default)
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

A16 Swap Override Strap

PCI_GNT#3	Low= A16 swap override Enable High= A16 swap override Disable
-----------	--



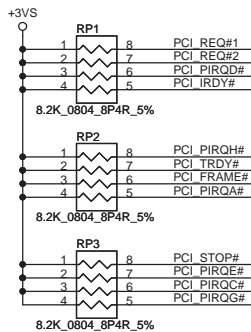
Danbury Technology Enabled

NV_ALE	High = Enabled Low = Disabled (Default)
--------	--

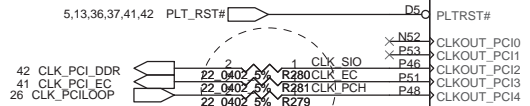
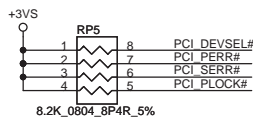
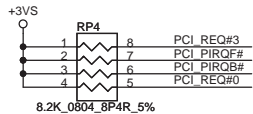
DMI Termination Voltage

NV_CLE	Low= Set to Vss (Default) High= Set to Vcc
--------	---

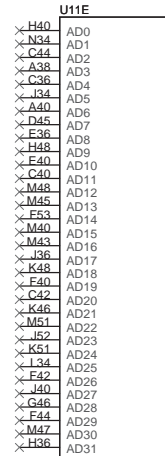
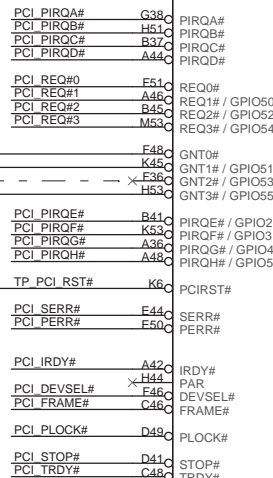
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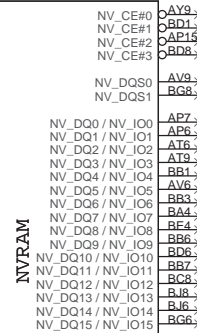
GNT2#: Not pull low, internal pull up 20K



Change to 47 ohm?



PCI



NVRAM

PCI

USB

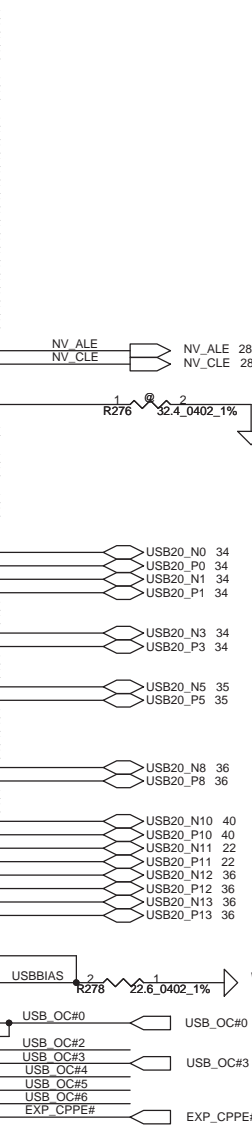
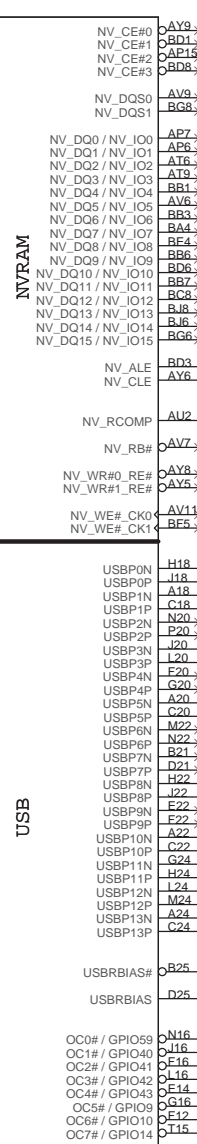
USB

USB

USB

USB

USB



USB-RIGHT1
USB-RIGHT2

eSATA-USB

BT

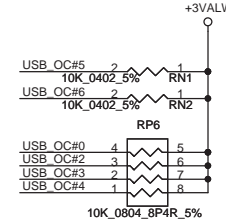
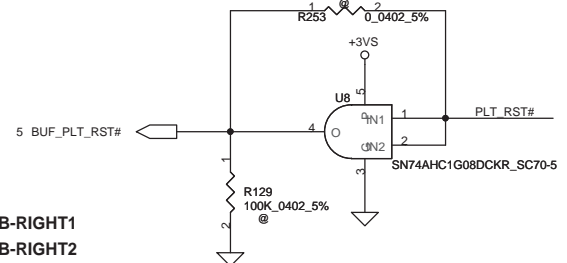
NewCard

Card reader(3 in 1)

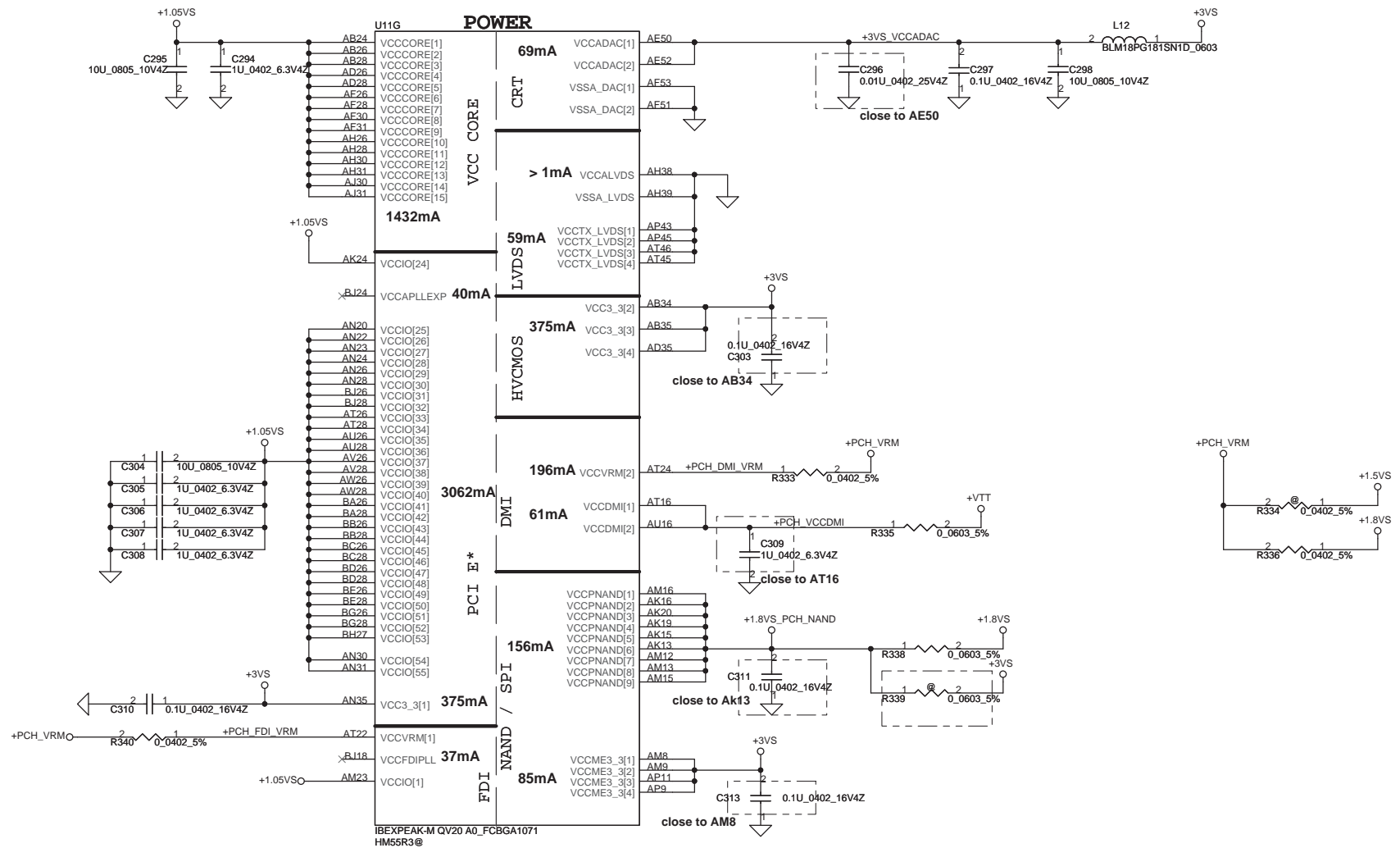
Int. Camera

3G

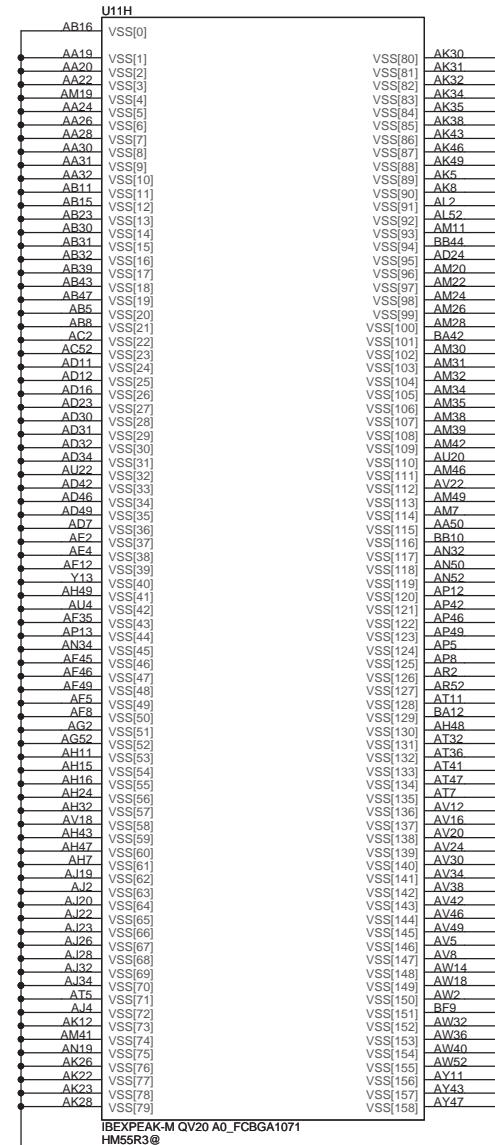
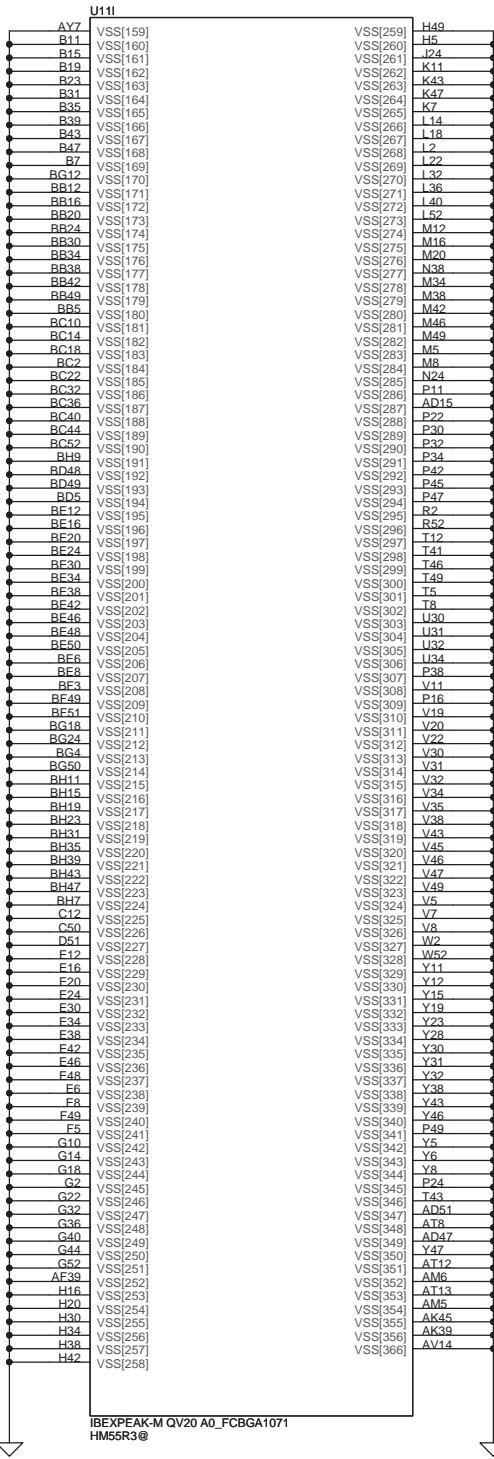
WiMax(WLAN)



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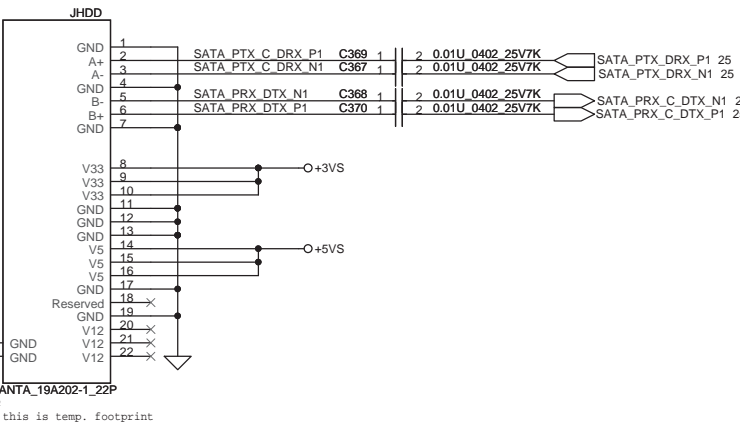
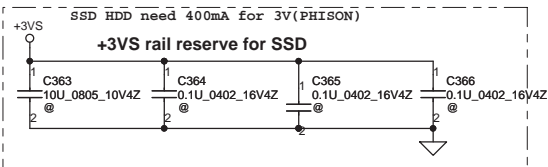
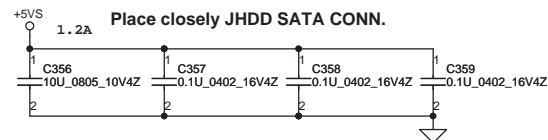


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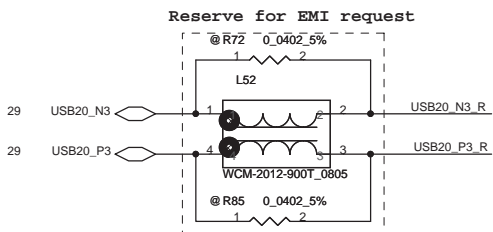
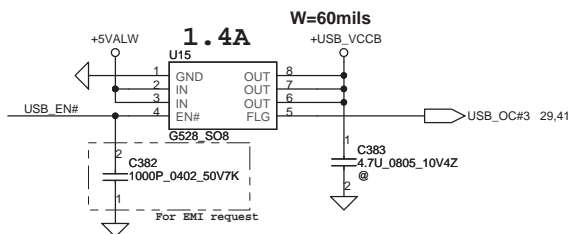


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SATA HDD Conn.

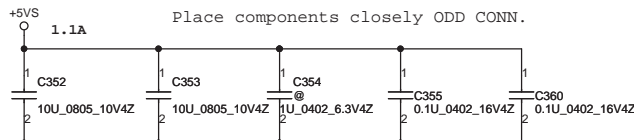


eSATA/USB

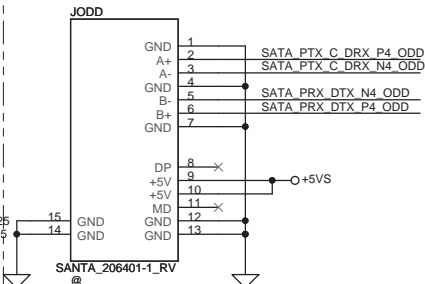


25 SATA_PT_X_DRX_P5
25 SATA_PT_X_DRX_N5
25 SATA_PR_X_C_DTX_N5
25 SATA_PR_X_C_DTX_P5

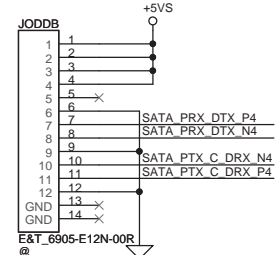
SATA ODD Conn



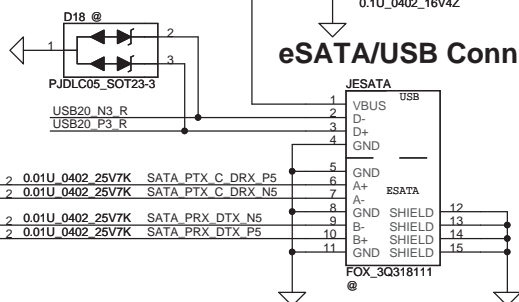
for 16" use



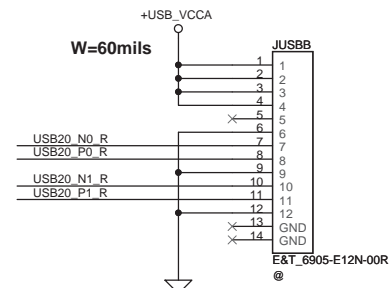
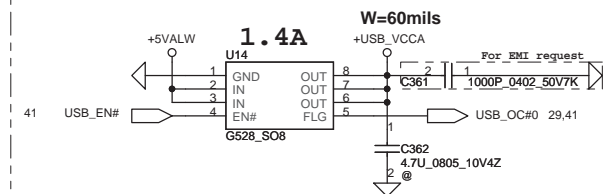
for 17" expansion using



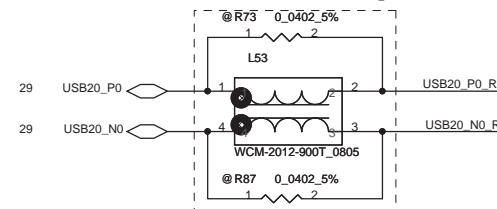
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SATA_PT_X_C_DRX_N4_ODD C372 1 2 16@ 0.01U_0402_25V7K
SATA_PR_X_DTX_N4_ODD C373 1 2 16@ 0.01U_0402_25V7K
SATA_PR_X_DTX_P4_ODD C374 1 2 16@ 0.01U_0402_25V7K
SATA_PR_X_DTX_P4 C375 1 2 17@ 0.01U_0402_25V7K
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SATA_PT_X_C_DRX_N4 C377 1 2 17@ 0.01U_0402_25V7K
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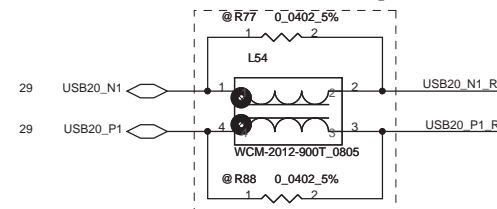
USB Board



Reserve for EMI request

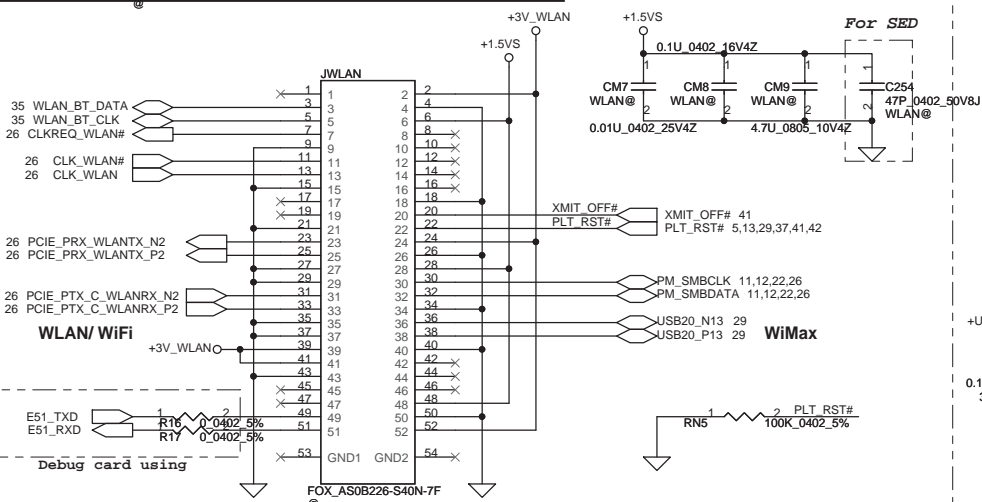
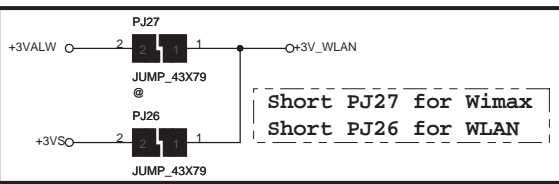


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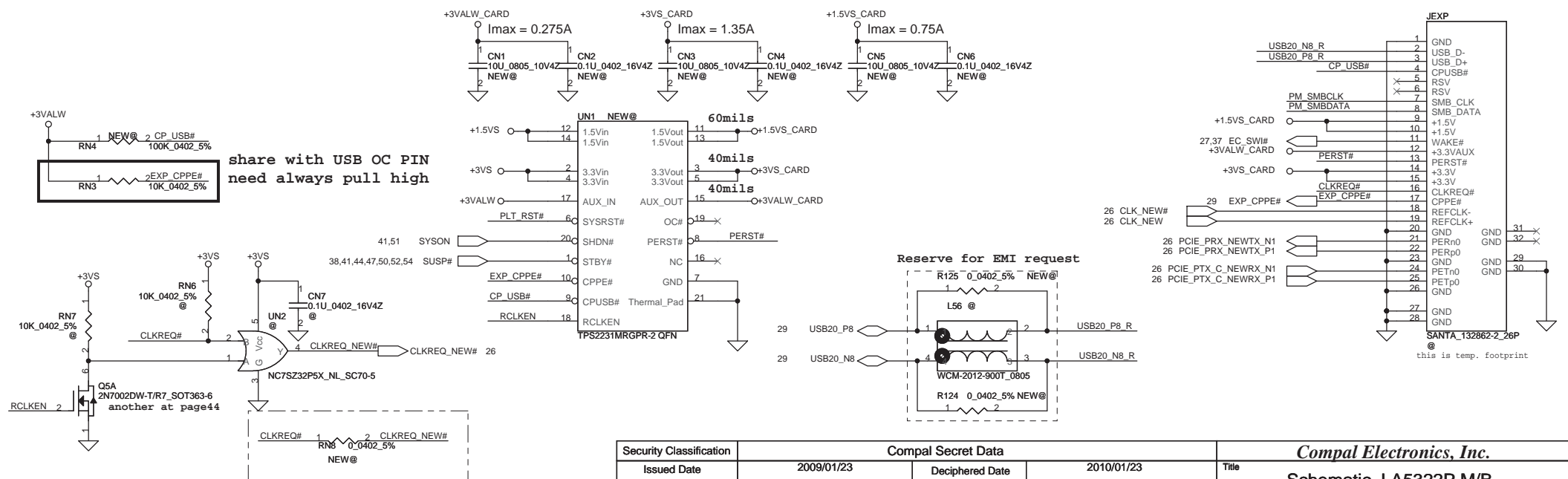
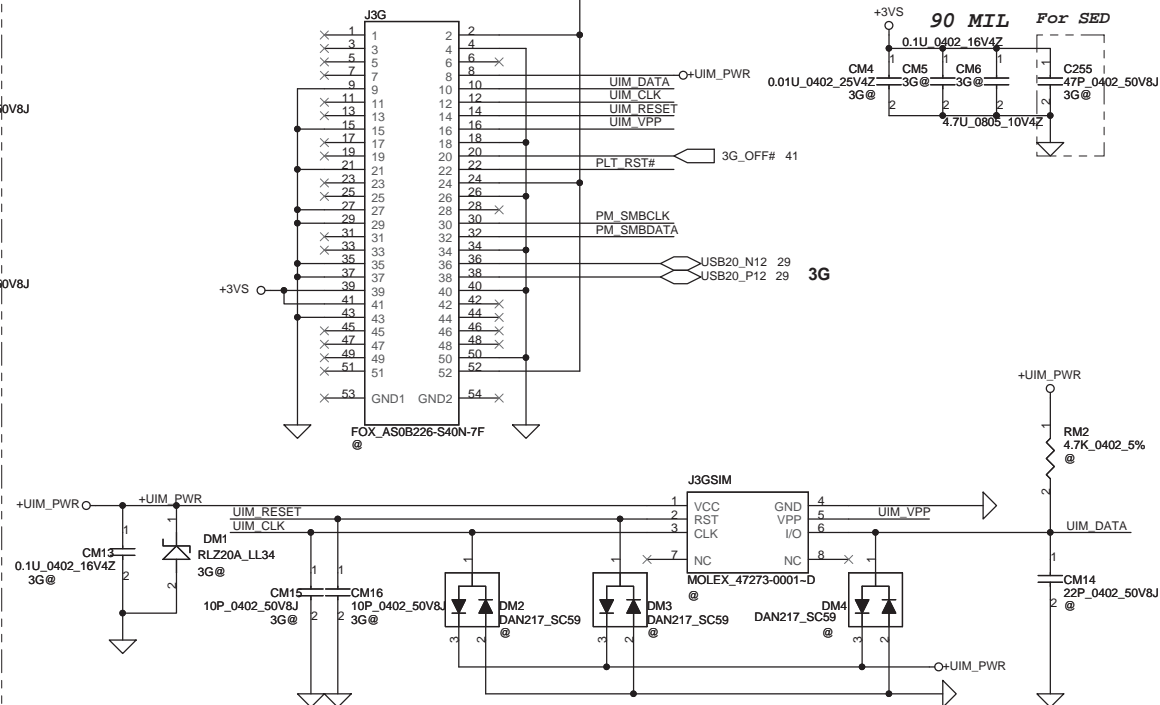


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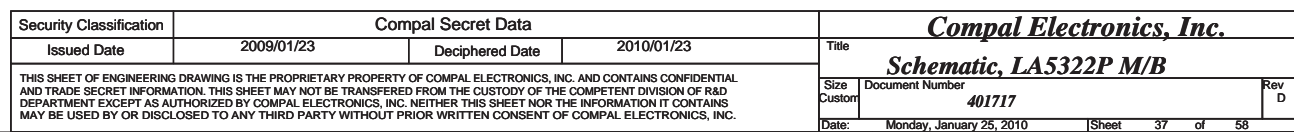
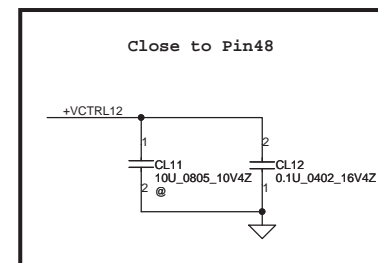
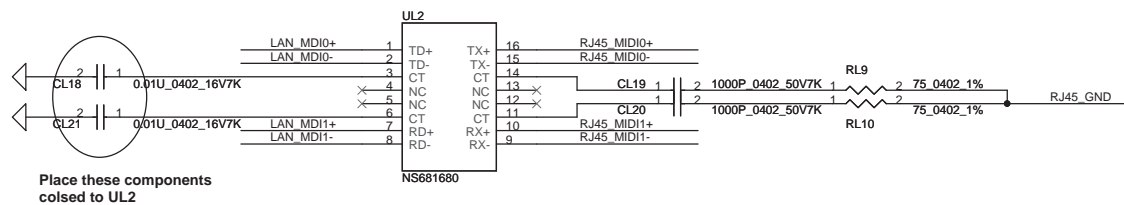
PCIe Mini Card-WLAN/WiMax



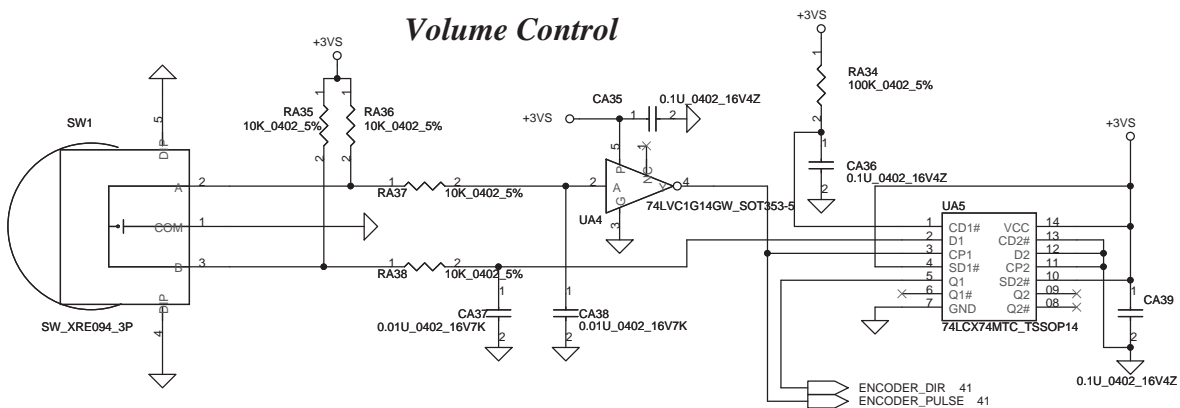
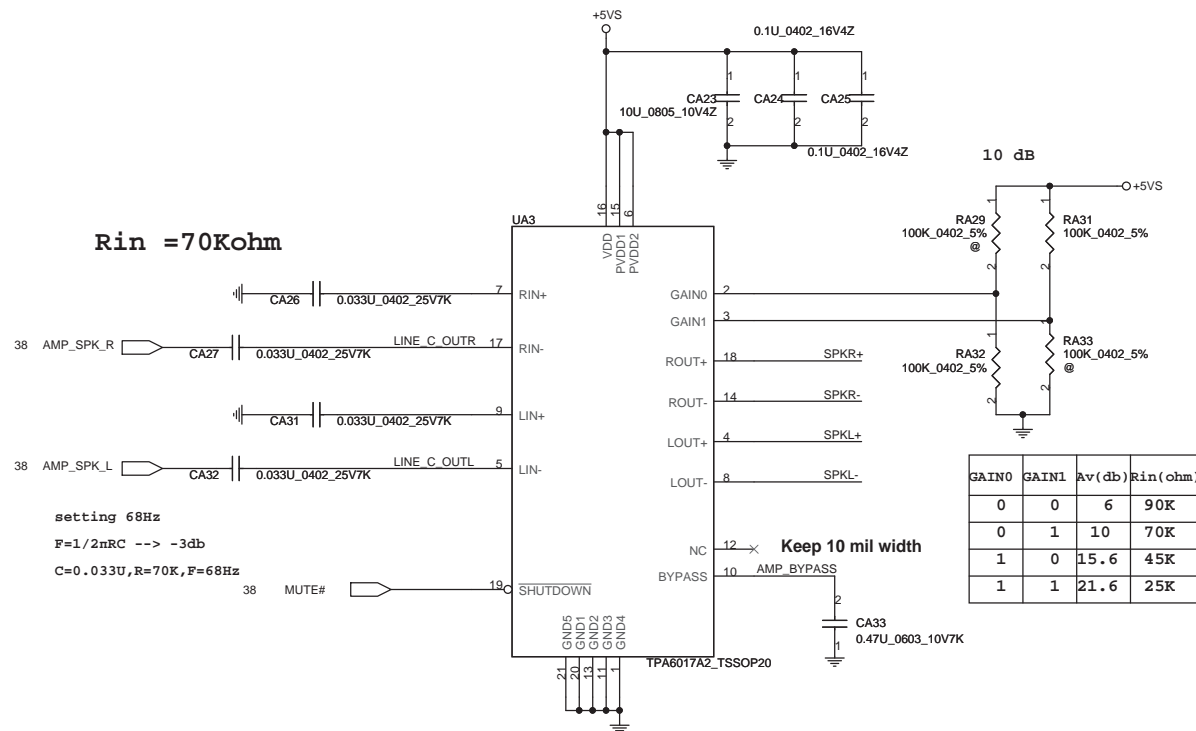
PCIe Mini Card-3G



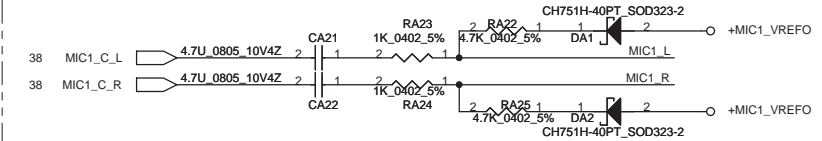
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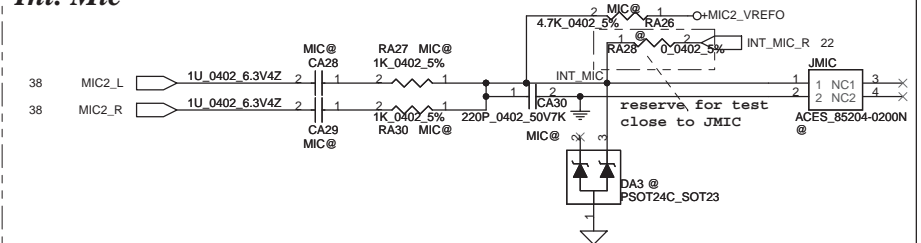
TPA6017 Medium Range Amplifier



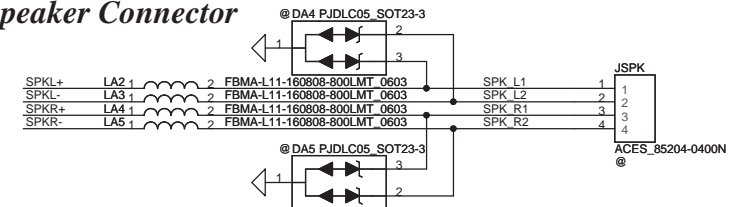
Ext. Mic



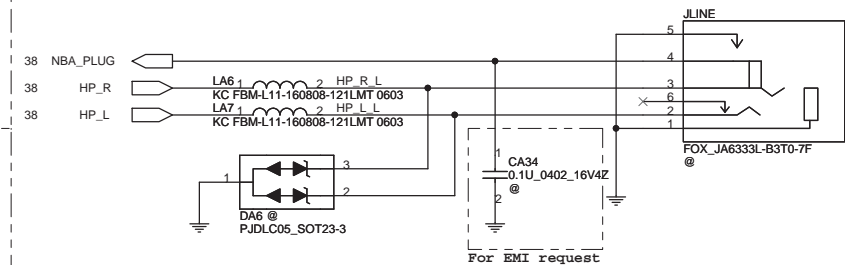
Int. Mic



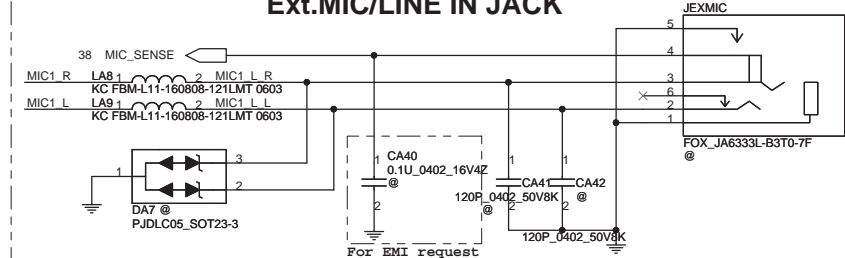
Speaker Connector



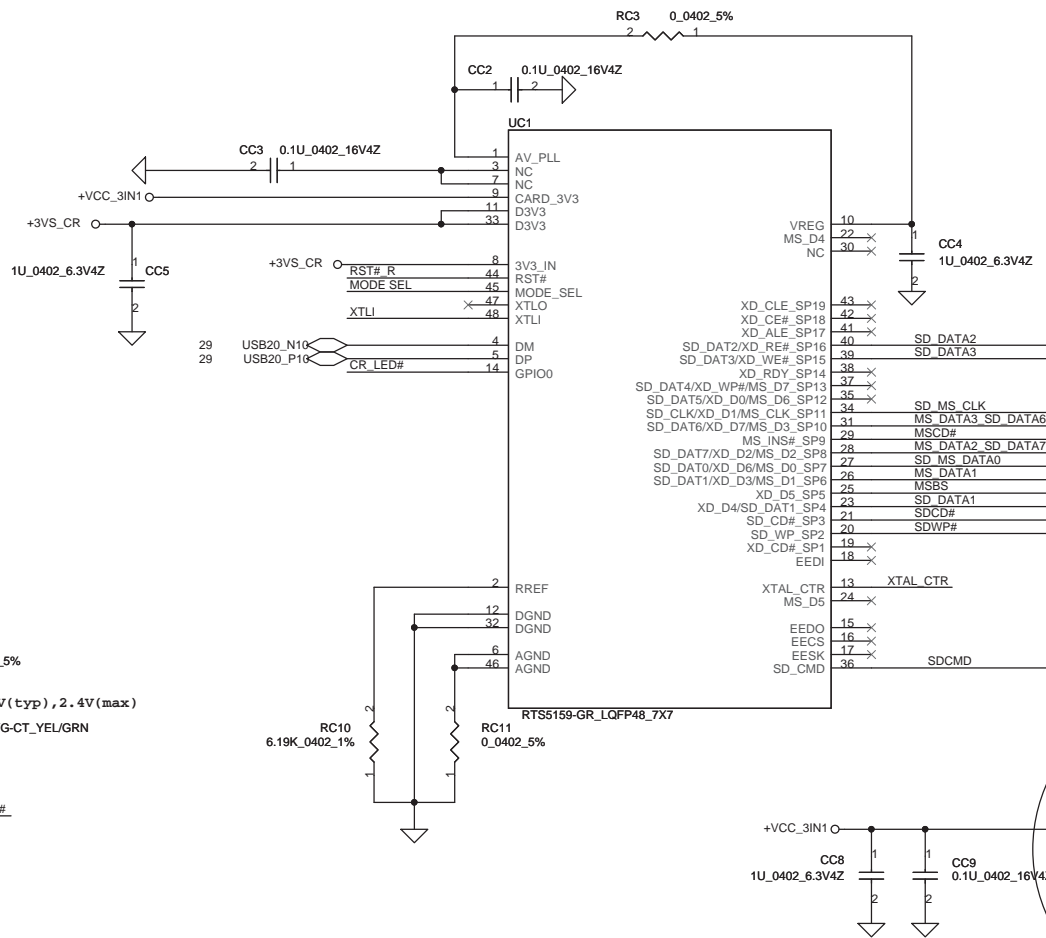
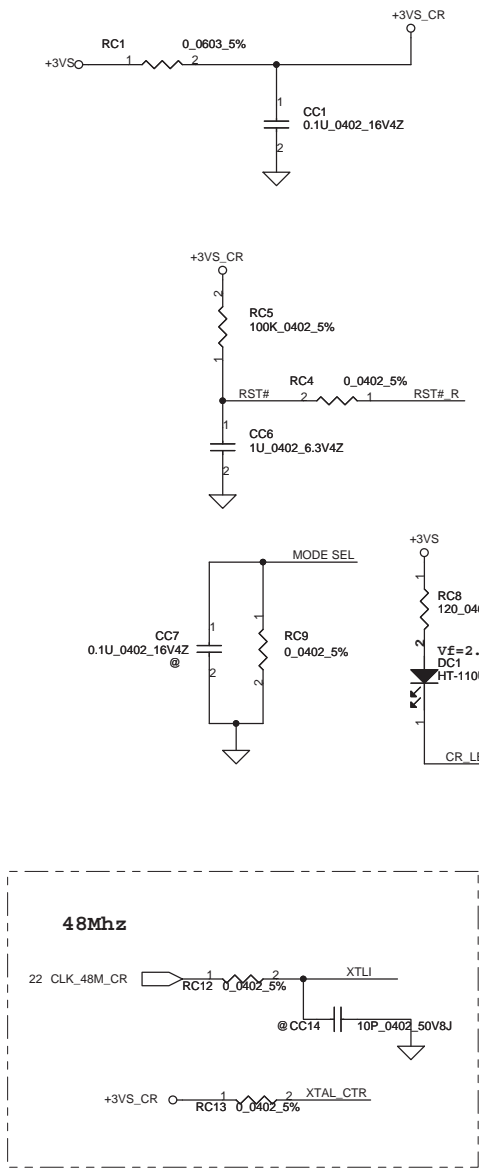
HeadPhone/LINE Out JACK



Ext.MIC/LINE IN JACK

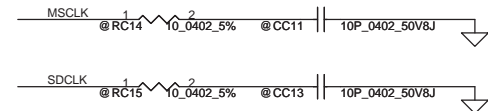
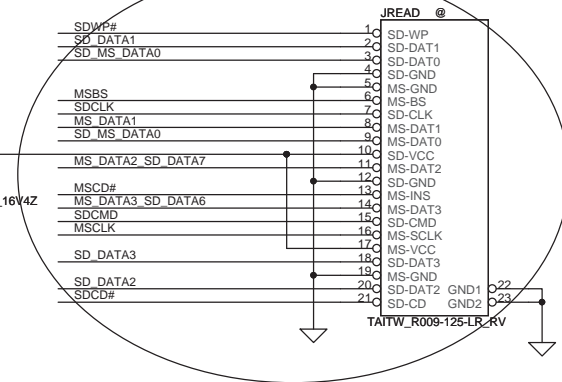


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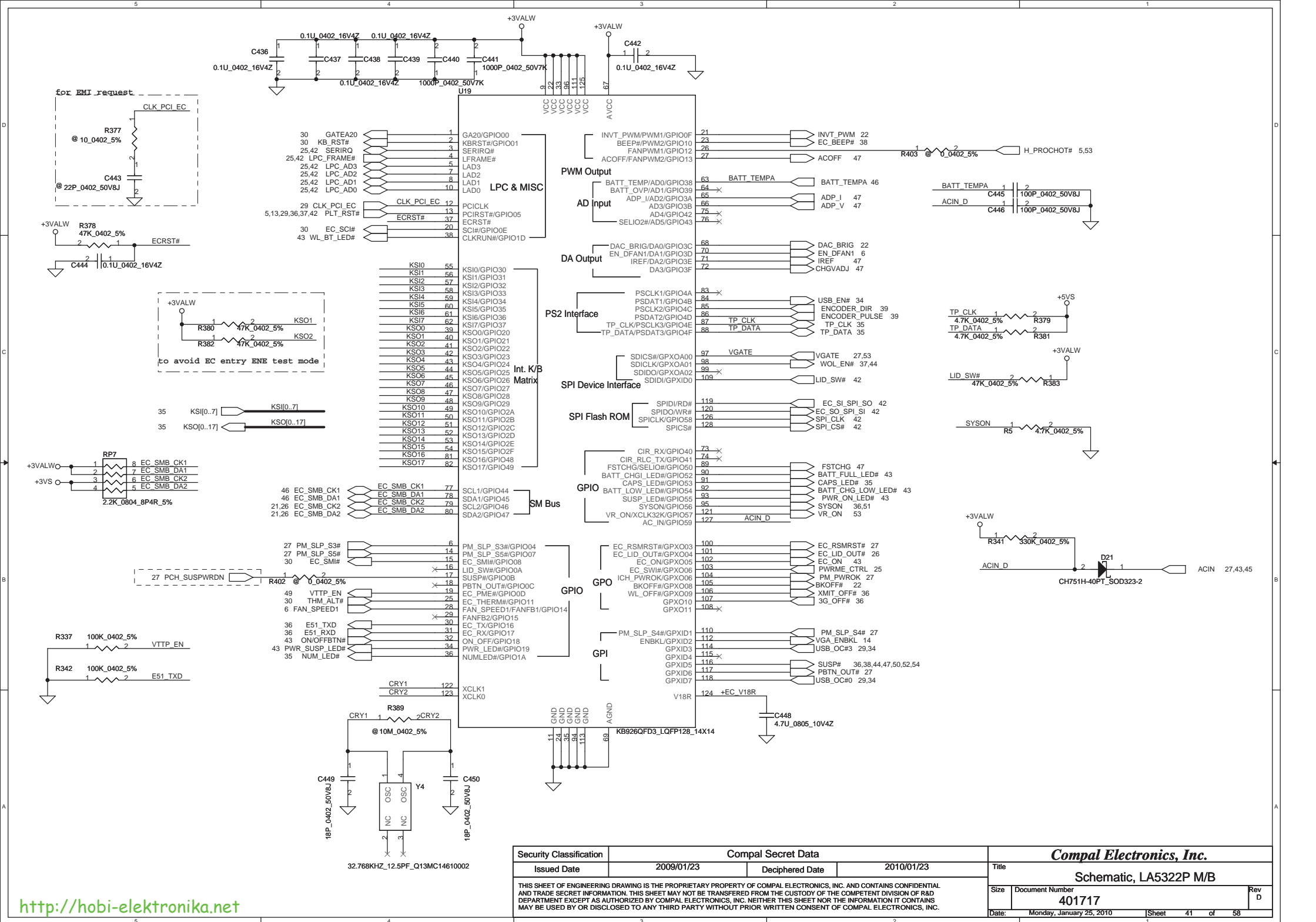
3 in 1 Card Reader

confirm all pin define with connector spec.

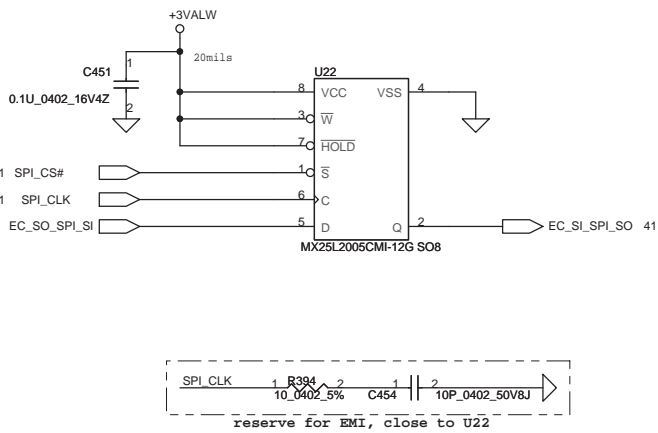


R	C	USB AUTO DE-LINK	MS FORMATTER	Description
0	NC	YES		Recommended
NC	47P	YES	YES	
NC	NC			Compatible with RTS5158E
NC	680P	YES		LED ON
10K	180P			LED ON
10K	680P		YES	

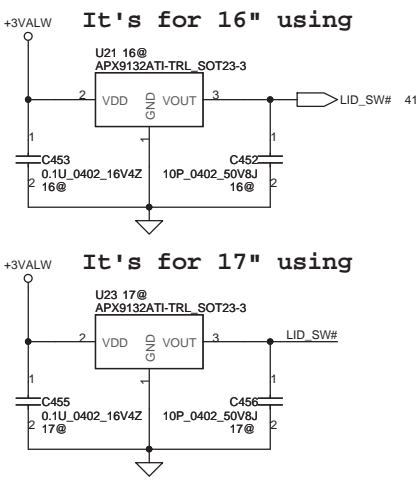
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SPI Flash (256KB)
Socket: SP07000F500 & SP07000H900

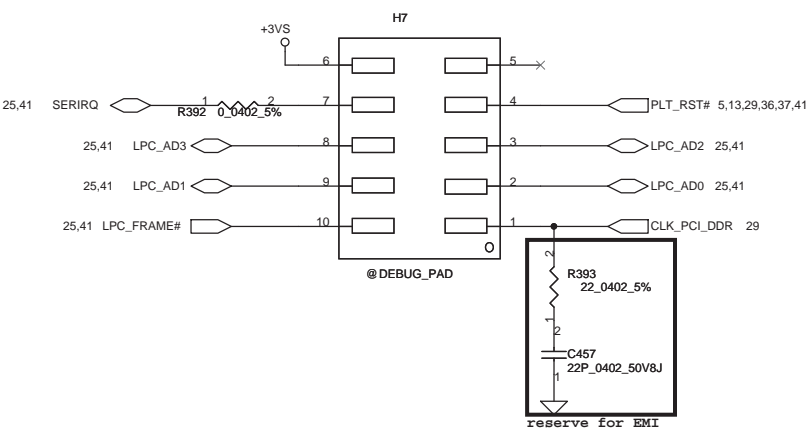


Lid SW



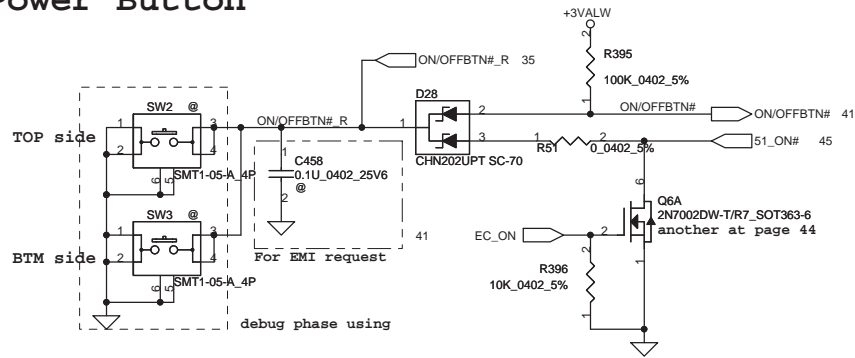
LPC Debug Port

Please place the PAD under DDR DIMM.

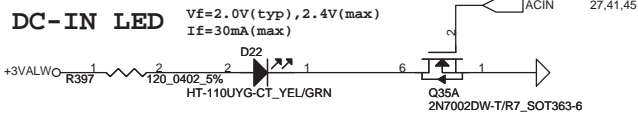
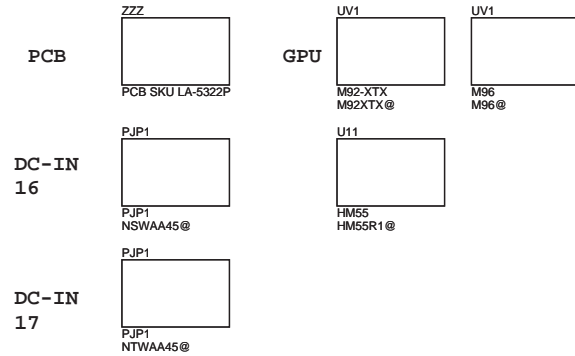


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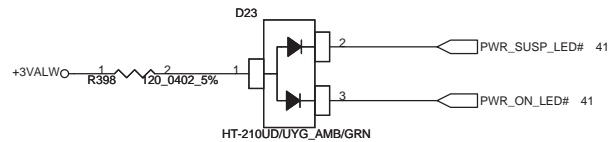
Power Button



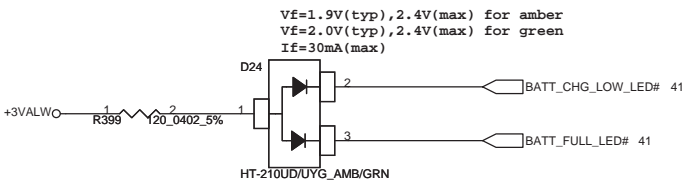
ISPD



POWER/SUSPEND LED



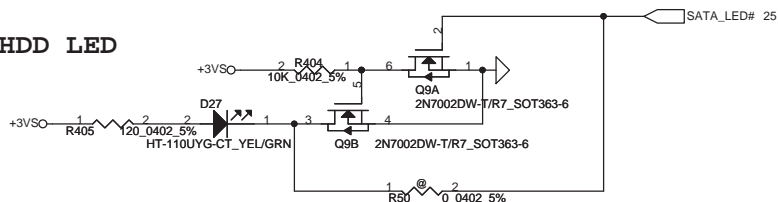
BATT CHARGE/FULL LED



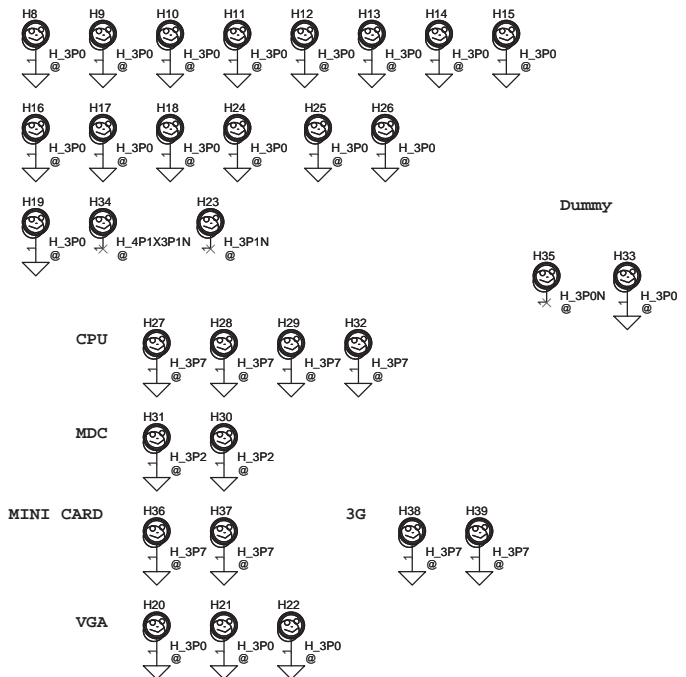
WL&BT LED



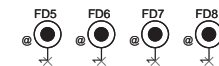
HDD LED



Screw Hole

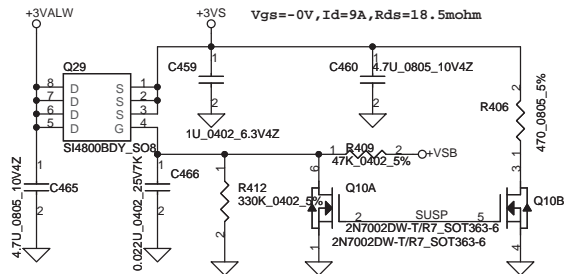


PCB Fedical Mark PAD

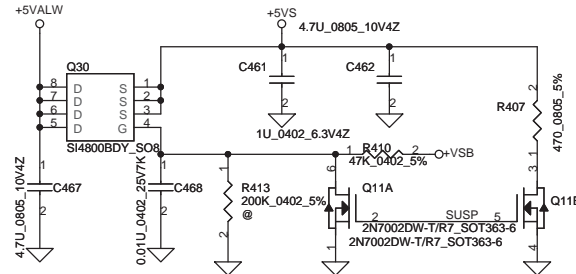


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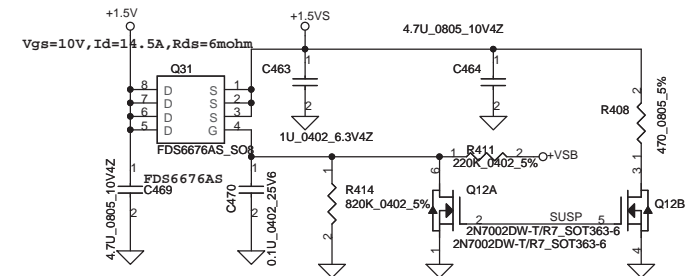
+3VALW TO +3VS



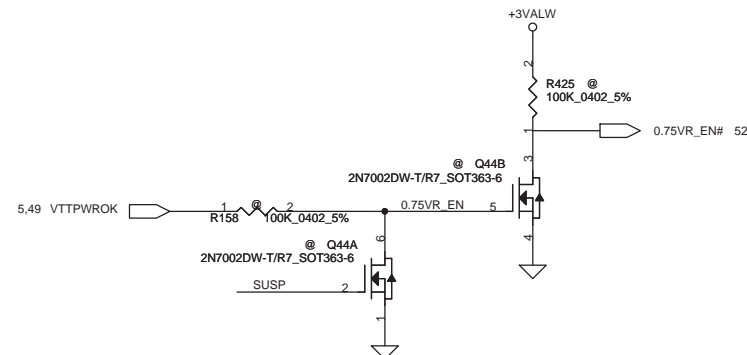
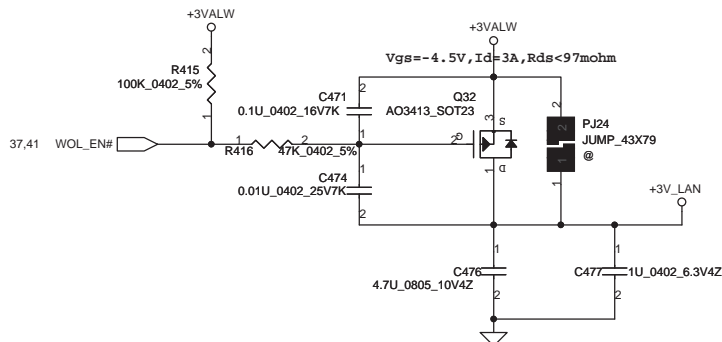
+5VALW TO +5VS



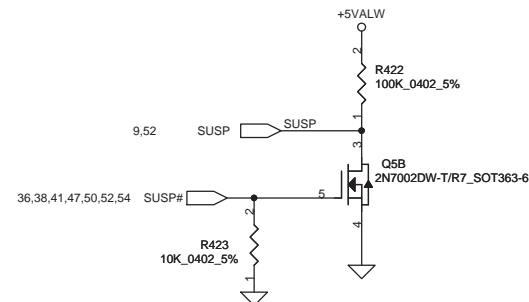
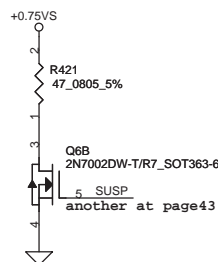
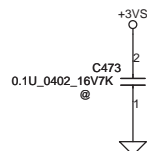
+1.5V to +1.5VS



+3VALW TO +3V_LAN

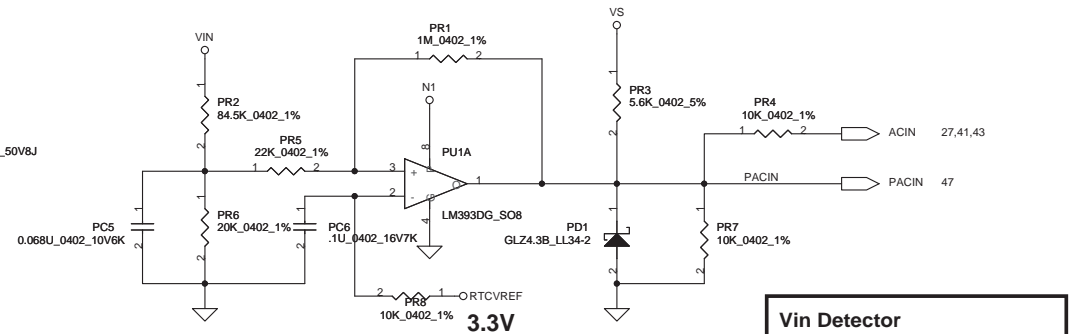
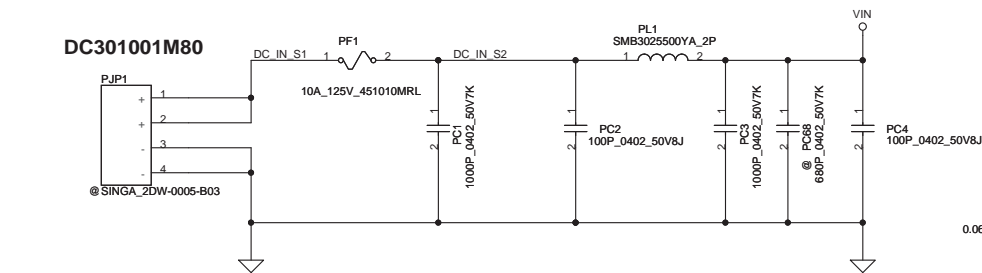


Reserve for EMI request



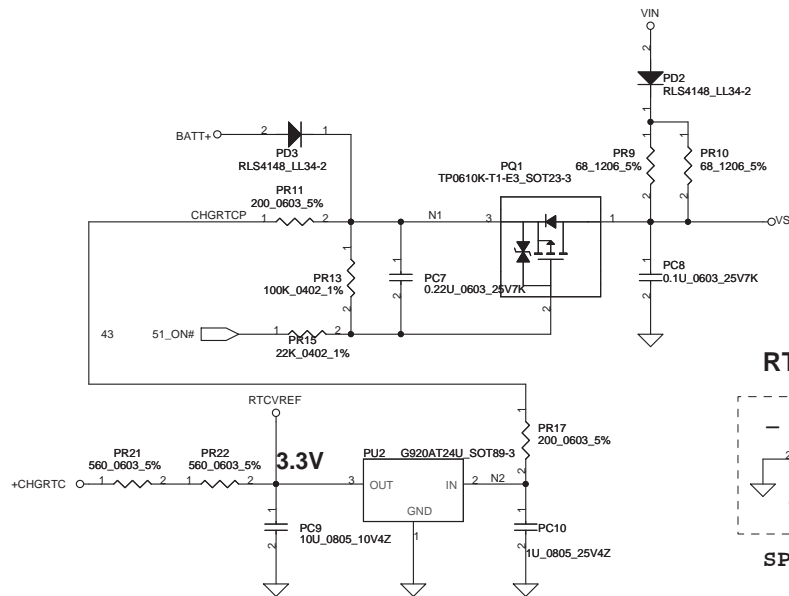
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DC301001M80

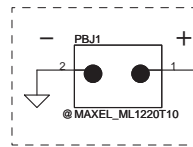


Vin Detector

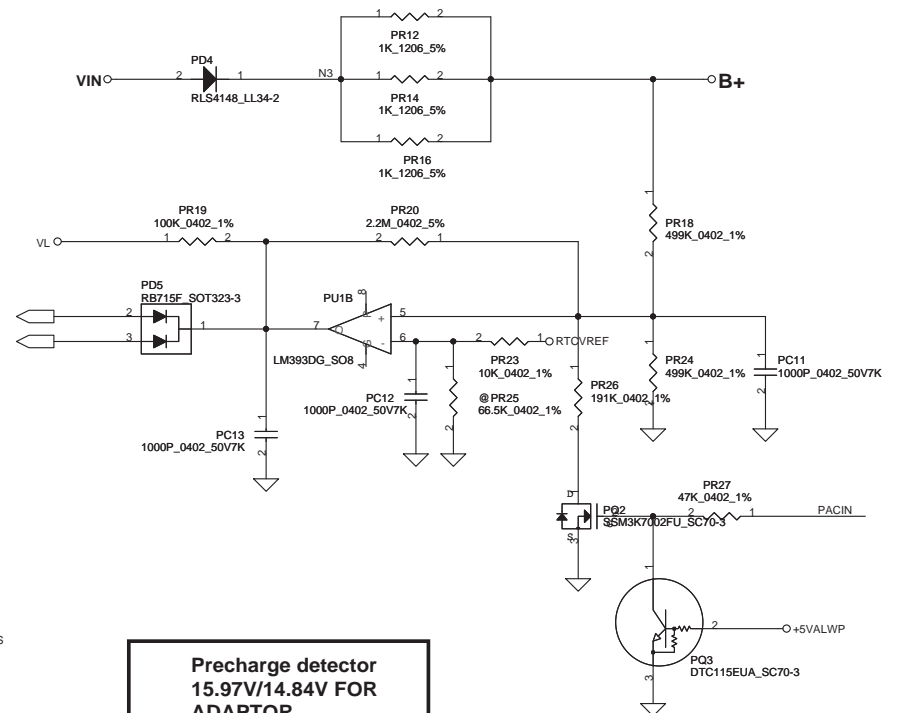
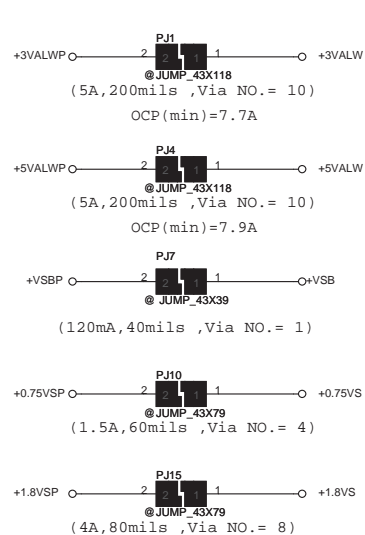
High 18.384 17.901 17.430
Low 17.728 17.257 16.976



RTC Battery



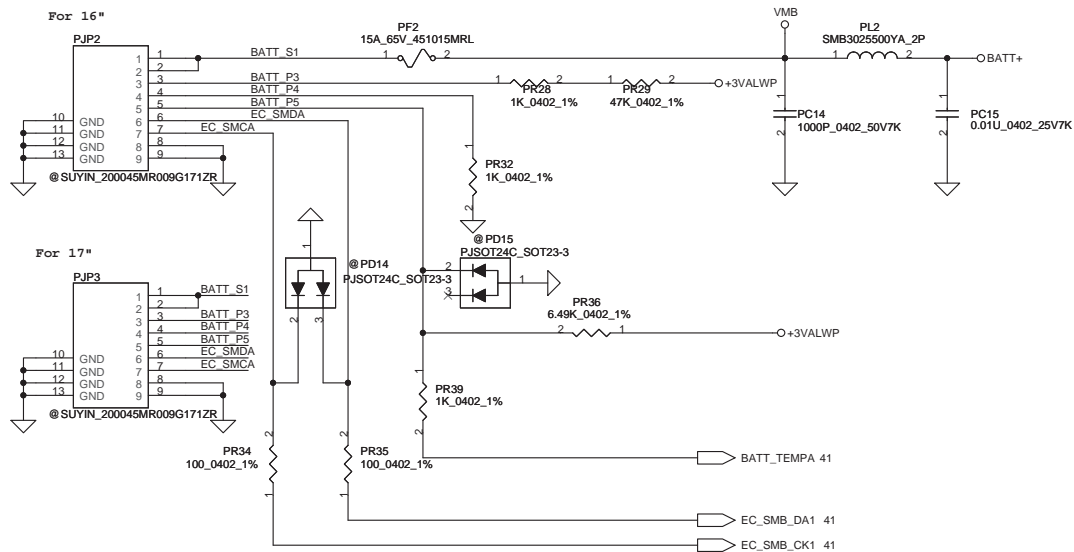
SP093MX0000



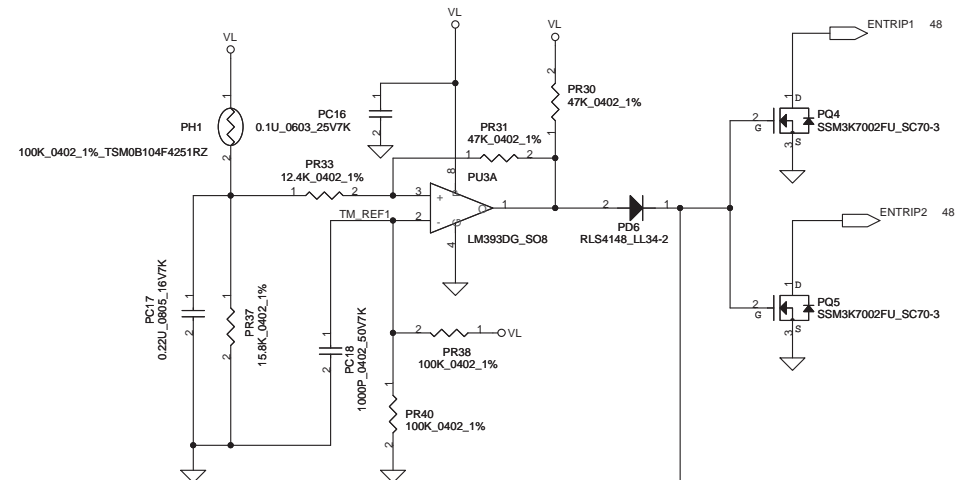
Precharge detector 15.97V/14.84V FOR ADAPTOR

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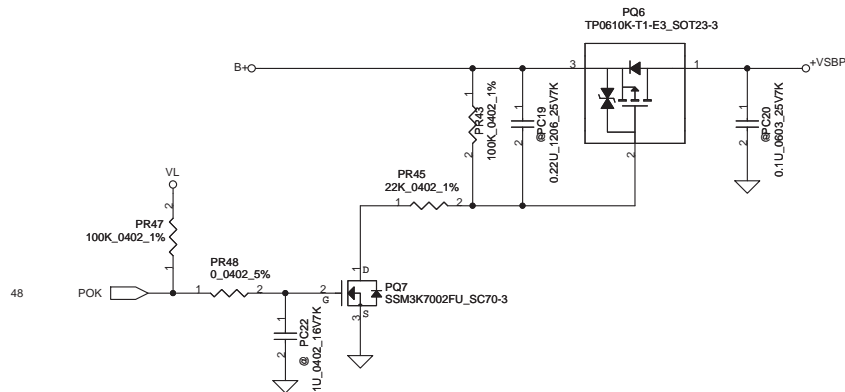
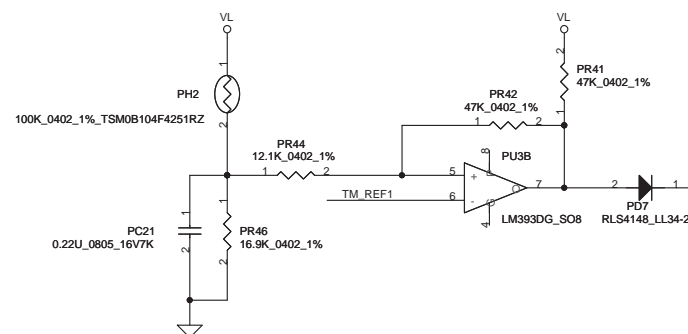
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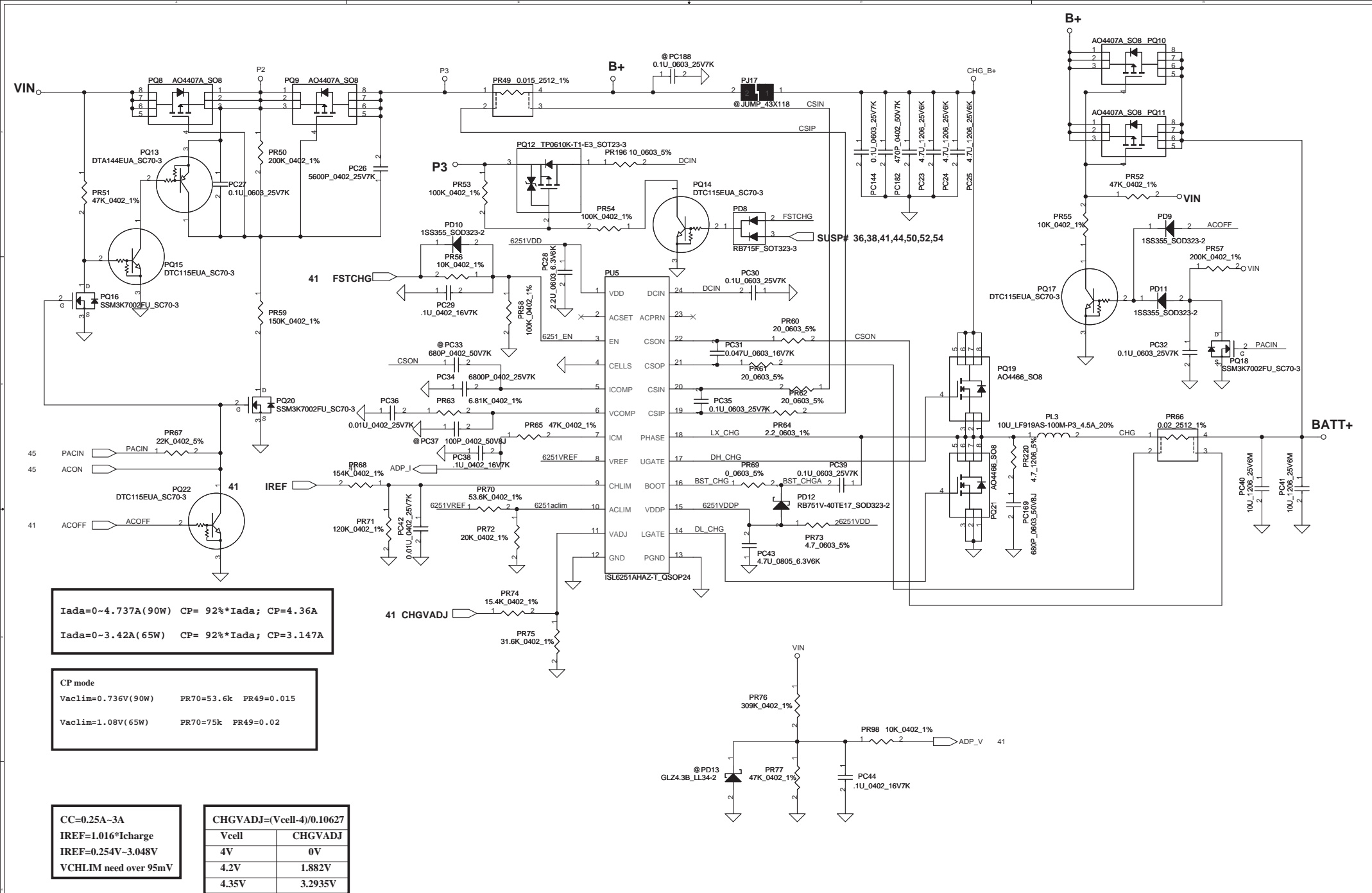
PH1 under CPU bottom side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C

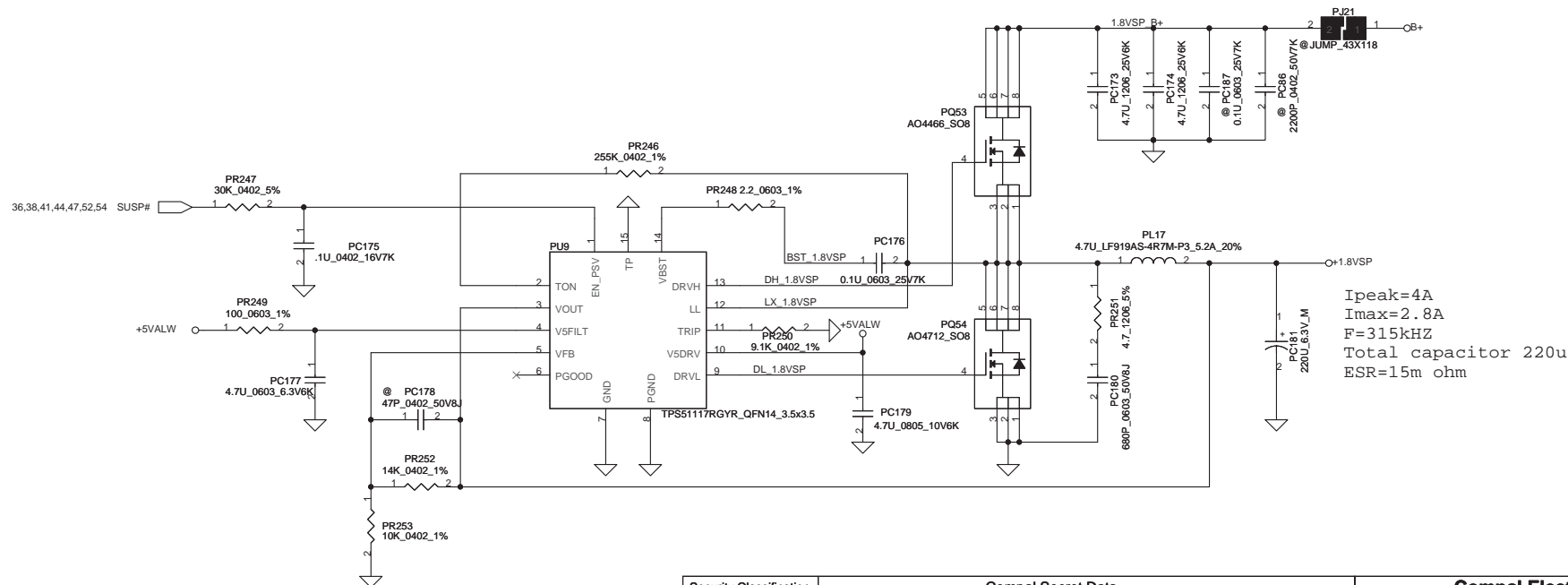
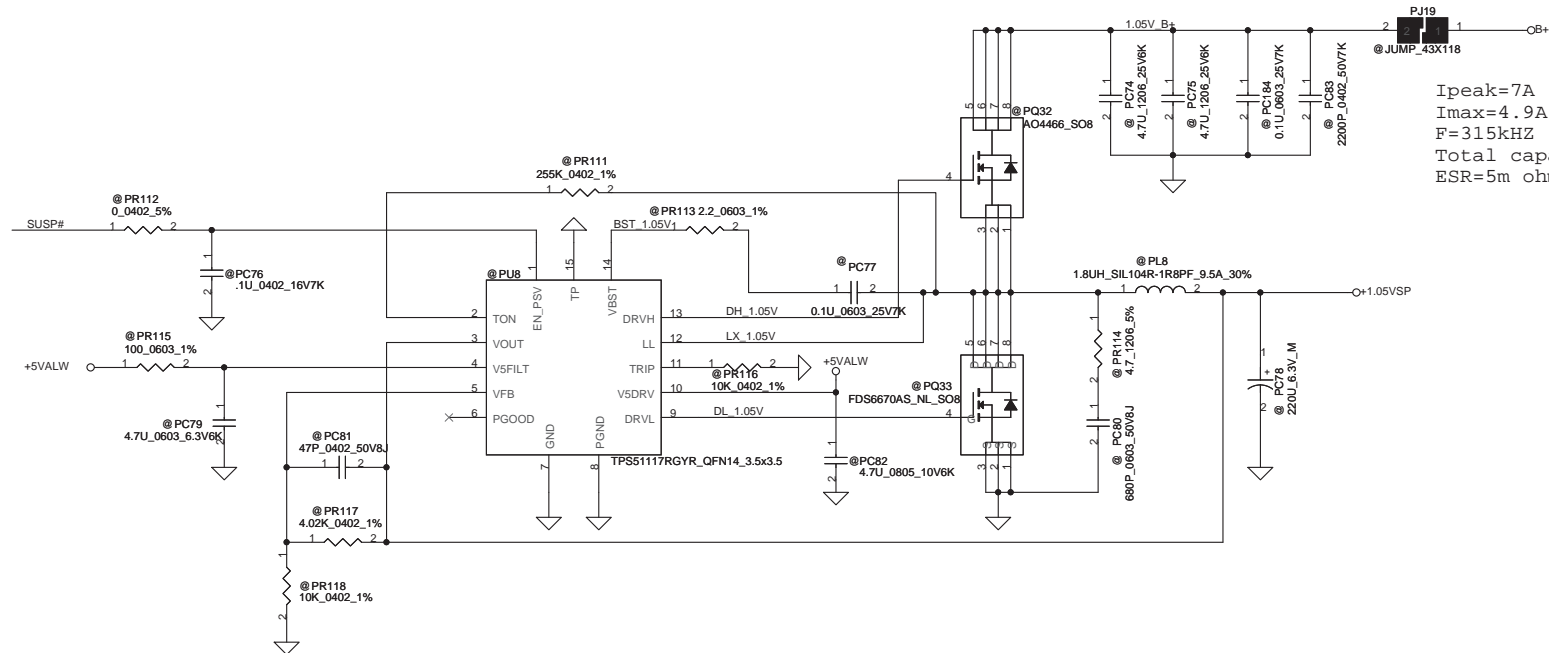


PH2 near main Battery CONN :
BAT. thermal protection at 90 degree C
Recovery at 55 degree C

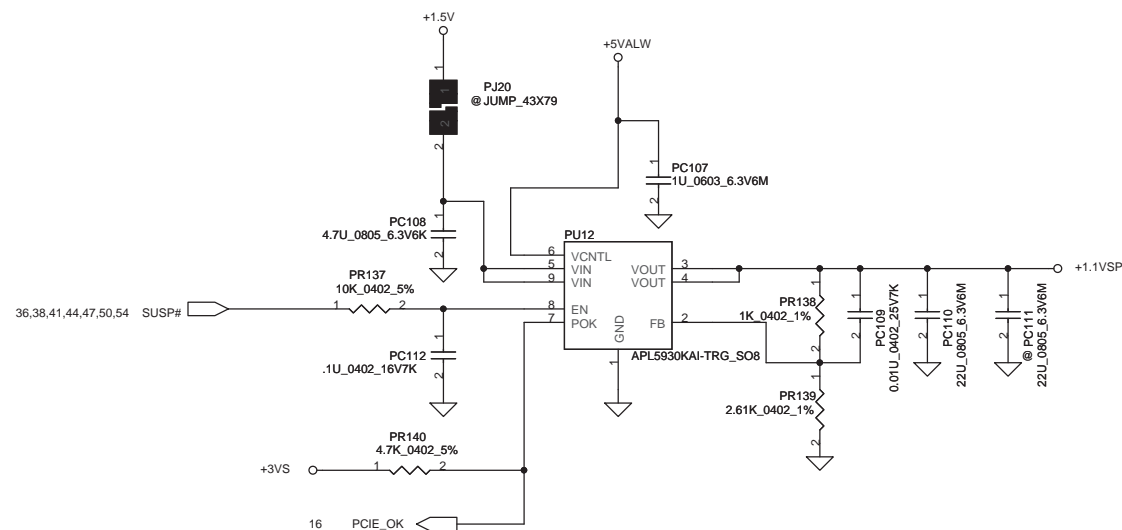
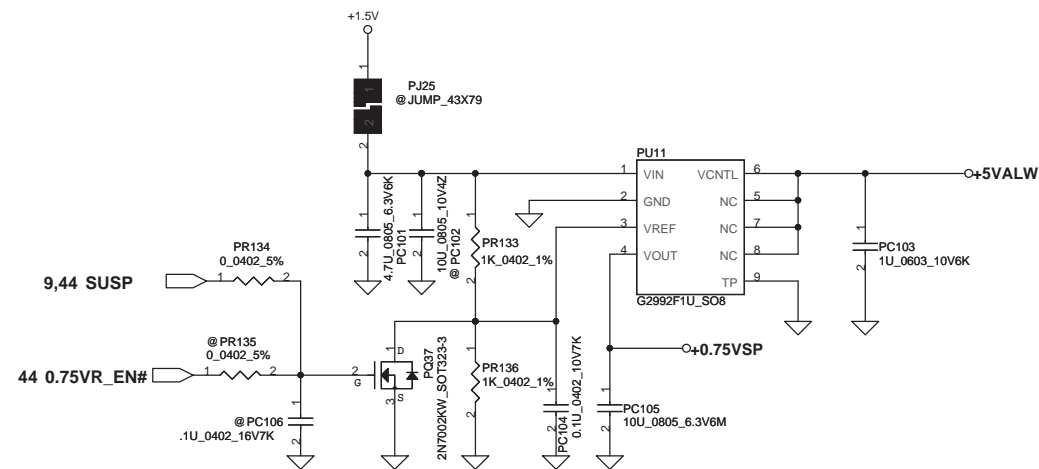


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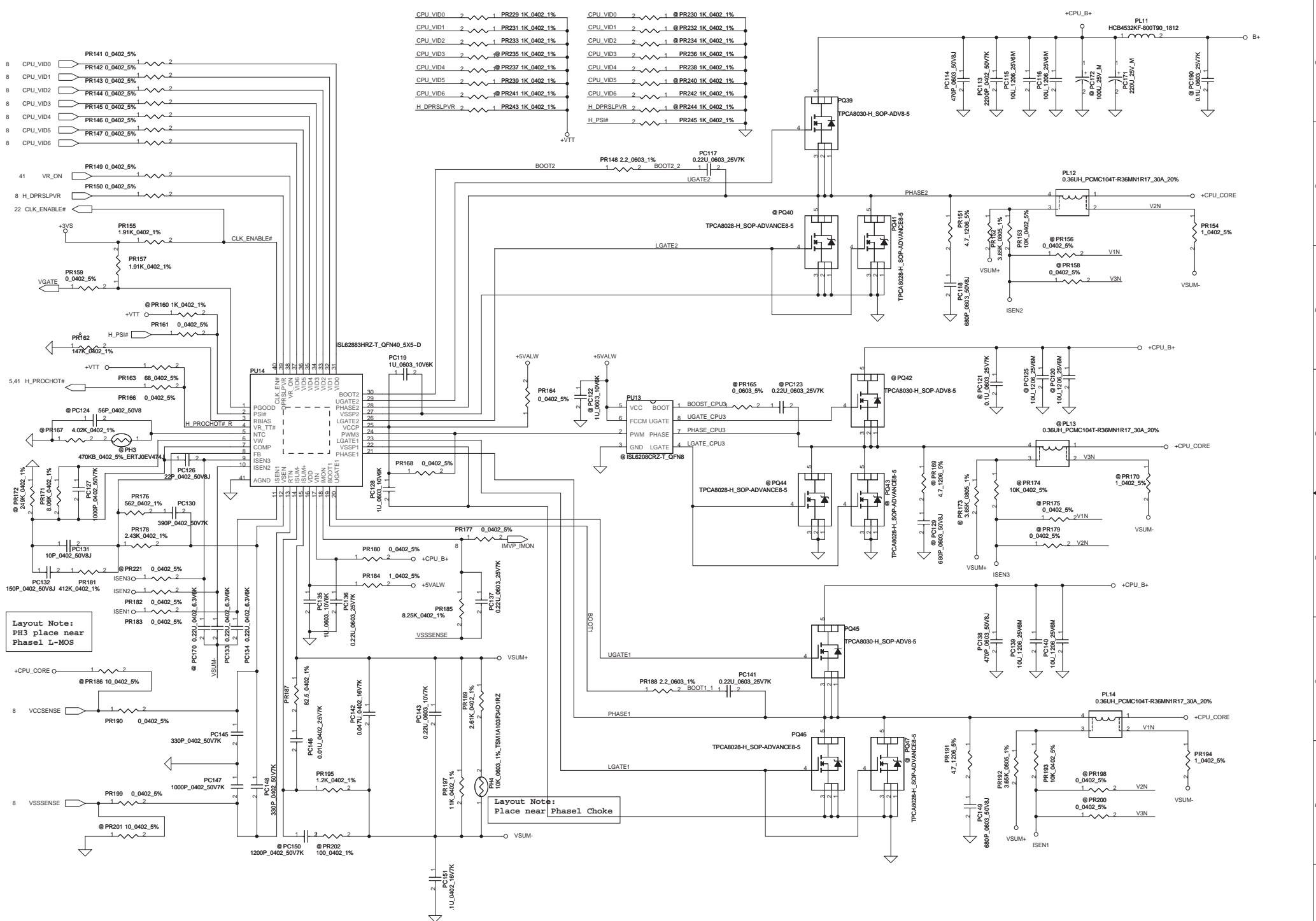


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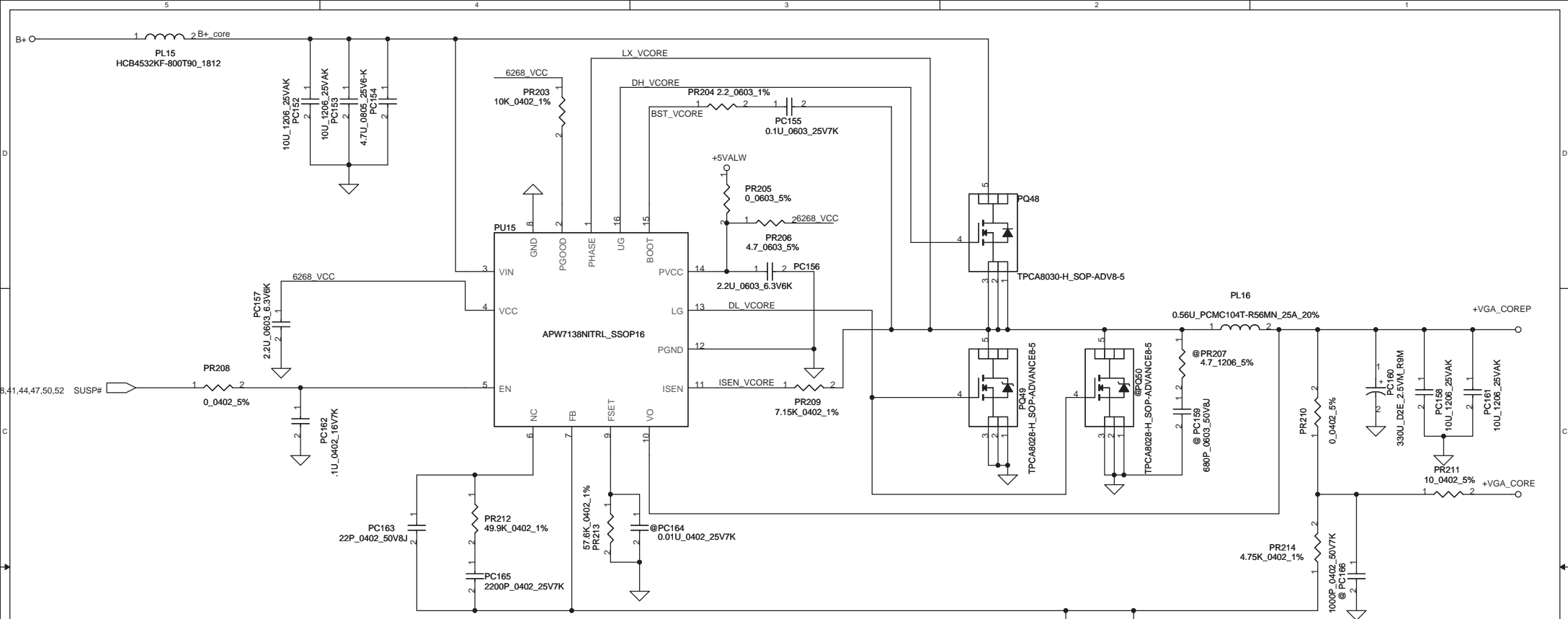


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$$VFB(0.6) = V_{out} \cdot R_{bottom} / (R_{top} + R_{bottom})$$

	M96	M92
VGA_PWSELECT	Core Voltage Level	Core Voltage Level
High	0.98 V	0.98 V
Low	1.1 V	1.2 V
resistor setting	PR214 = 4.75K PR218 = 7.5K PR215 = 23.7K	PR214 = 4.75K PR218 = 7.5K PR215 = 13K

$$FSW = 1 / (75E-12 \cdot 57.6K) = 231.48KHz$$

M96	M92
Imax=18.23A Ipeak=26.05A Iocp=28.65A	Imax=12.81A Ipeak=18.30A Iocp=20.14A
PR209=7.15K PQ50=unpop	PR209=5.36K PQ50=unpop

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PIR (Product Improve Record)

NSWAA LA-5322P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.1 TO 0.2

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
3/25	31, 32		DEL L14,C302,L15,C312,L16,C314,C315,L19,C339,C340	DG1.5: these pins have internal VRM

NSWAA LA-5322P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.2 TO 0.3

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
6/29	11		Add R92,R93	To support M1 mode
6/29	27		Change R324 from 10K to 330K	To solve ACIN LED issue
7/02	30		Change BT_PWR# from GPIO0 to GPIO34, add VGA_HDMI_HPD on GPIO0.	For common design with NSKAA
7/02	35		DEL JCAM (R431,R432,C403,R371,R373,R374,R375,L20)	CAM cable combine with LVDS
7/02	22		DEL R387	Remove +5VALW power to camera
7/02	40		DEL YC1,CC10,CC12	Remove 12MHz crystal to cardreader
7/02	40		DEL RC2	Remove +3VALW to cardreader
7/02	15~18		Add LV31,CV253,CV236,CV270,LV35,LV36,CV303,CV304, CV305,CV306,CV307,CV308,LV34,RV157,RV156,RV24,RV56 RV59,RV60,RV126,RV127	Reserve for support Park/Madsion
7/03	22		Add R120,R401	Reserve +1.5VS to clk gen for low power clk gen test
7/03	22,30		Add R154	Reserve LVDS_SEL on PCH GPIO45
7/03	30,41		Connect PCH GPIO33 to EC pin 103 as PWRME_CTRL Change 3G_OFF# from EC pin 103 to pin 107	To reflash ME BIOS
7/17	43		Add R50 on SATA_LED#	Reserve for cost down plan
7/17	29		DEL R277,D12, Connect USB_OC#3_D to USB_OC#3	
7/17	27,41,43		DEL R384, D14. Add R331	Modify ACIN circuit
7/17	22,43		Change Q7,Q34 to Dual Q35	For cost down
7/20	5,9,11, 30,44		Add Q41,R19,R123,R22,D54,U10,R33,R52,Q33,R424,R417, C179,Q46,C472,R417,R418,C205,C186,C185,C180,PJ30,PJ31, R80,Q44,R425,R158,Q39,Q40,R94,R95,R122,R121 Add RST_GATE on PCH GPIO46	Reserve S3 power reduction circuit
7/27	41		Add R5	To solve SYSON glitch issue
7/27	30,41		Connect PCH GPIO49 to EC pin25 as THM_ALT#	Reserve for test
7/27	8,9,11, 16,20		Add C144,C159,C218,C216,C217,CV309,CV310,CV311,CV312	For cost down
7/30	9,44		Add C160,C256,C257,C258,C473,C475	For EMI request
7/30	25,42		Change U13 to 8MB, U22 to 1MB	For SW and EC request

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PIR (Product Improve Record)

NSWAA LA-5322P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.3 TO 0.4

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
8/19		14,22	Add R159,R160 for VGA BKL control	Reserve for deep green test
9/1			Change +3VL to +3VALW, DEL PJ12	.
9/1		25,42	Change EC ROM to 256KB and PCH ROM to 4MB	For PVT test
9/1		34	Add L52,R72,R85,L53,R73,R87,L54,R77,R88	For EMI request
9/9		37	Connect WOL_EN# to LAN IC	For PVT test

NSWAA LA-5322P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.4 TO 1.0

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
9/30		25	Change C287,C290 from 18p to 15p	To fine tune RTC timing
9/30		5	Change R22 from 10k to 1k	Modify S3 circuit
10/28		5	Reserve C301,C384,C389	Reserve for S3 power saving circuit

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NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
EVT		P47-PWR_CHARGER	Change PR65 100 to 47k	For CPU throtting setting (2009/05/20)
EVT		P48-PWR_3VALWP/5VALWP	Change PR81 19.6k to 19.1k	modify +5VALWP voltage to 5.14V (2009/05/20)
EVT		P49-PWR_+1.1V_VTTP	Add PR290 100K, PR291 180K, PR292 10K, PR293 4.7K, PR294 100K, PC228 0.01U, PC229 0.1U, PQ55,PQ56	Add switching circuit for H_VTTSELECT function (2009/05/20)
EVT		P49-PWR_+1.1V_VTTP	Change PR94 10K to 3.4K Add PR101 1K	Set VTTPPWROK voltage level to 1.1V (2009/05/20)
EVT		P53-PWR_CPU_CORE	Remove PR186,PR201 10 Ohm	Modify CPU_CORE circuit (2009/05/27)
EVT		P46-PWR_BATTERY CONN / OTP	Change PH1,PH2 0603 sizt to 0402 size	For cost down (2009/05/27)
EVT		P50-PWR_1.05VSP/1.8VSP	Change PR115,PR249 422Ohm to 100 Ohm Change PC79,PC177 1U to 4.7U	avoid 2nd source RT8209B can no power on (2009/06/05)
EVT		P52-PWR_0.75VSP/1.1VSP	Change PU12 APL5913 to APL5930	For cost down (2009/06/05)
EVT		P45-PWR_DCIN/DECTOR	Remove DC301000F00	Remove DC IN JACK((2009/06/05))
EVT		P54-PWR_VGA_COREP	Change PR210 10 Ohm to 0 Ohm Change PR211 0 Ohm to 10 Ohm	Change VGA_CORE sense from HW terminal to PWR (2009/06/05)
EVT		P54-PWR_VGA_COREP	Change PL16 0.36U to 0.56U	Change CPU_CORE CHOKE to 0.56U(2009/06/05)
EVT		P50-PWR_1.05VSP/1.8VSP	Change PR116 14.7k to 10k Change PR250 15.4k to 9.1k	Set 1.05V OCP to 8.54A(2009/06/05) Set 1.8V OCP to 4.93A(2009/06/05)
EVT		P51-PWR_1.5VP	Change PR127 7.15k to 2.1k	Set 1.5V OCP to 17A(2009/06/05)
EVT		P49-PWR_+VTTP	Change PR99 5.9k to 2.43k	Change VTT OCP to 19.7A(2009/06/05)
DVT		P50-PWR_1.05VSP/1.8VSP	Add PC175 0.1U Change PR247 0 to 30k	For power sequence(2009/07/07)
DVT		P49-PWR_+VTTP	Change PR99 2.43k to 4.99k	Set OCP(2009/07/07)
DVT		P51-PWR_1.5VP	Change PR127 2.1k to 4.7k	Set OCP(2009/07/07)
DVT		P45-PWR_CPU_CORE	PC133, PC134 SE083224Z80 to SE124224K80	PC133, PC134 tolerance Y5V to X5R(2009/0/07)
DVT		P50-PWR_1.05VSP/1.8VSP	Change PC79, PC177 SE00000MAN0 to SE107475K80	Change part number(2009/07/07)
DVT		P41-PWR_3VALWP/5VALWP	Add PC87 1U_0402_6.3V6K	Avoid pre-charge can not finish(2009/07/07)
DVT		P41-PWR_3VALWP/5VALWP	Add PC45 0.22U to 1U	Prevent +3VALW/+5VALW can't boot up (2009/07/07)
DVT		P45-PWR_CPU_CORE	Change PR229-PR245 and PR160 10k to 1k	Change VID, PSI# and DPRSLPVR select resistor from 10k to 1k (2009/07/17)
DVT		P45-PWR_CPU_CORE	Change PR157 10k to 1.91k	Change PGOOD pull high resistor 10k to 1.91k(2009/07/17)
DVT		P45-PWR_CPU_CORE	Remove PH3, PC124, PR167 Change PC133, PC134, PC170 pin 2 from GND to VSUM- Change PR152, PR192 0402 size to 0805 size	Modify circuit for CPU_CORE(2009/07/17)
DVT		P39-PWR_BATTERY CONN / OTP	Change +3VLP to +3VALWP	Remove +3VLP power rail (2009/07/17)

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NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
DVT			P47-PWR_CHARGER	Reserve PC188 0.1U
DVT			P49-PWR_VTTP	Reserve PC189 0.1U
DVT			P49-PWR_VTTP	Change PR95 0 ohm to 2.2 ohm
DVT			P49-PWR_VTTP	Add PR100 4.7 ohm, PC70 680P
DVT			P49-PWR_VTTP	Change PR94 3.4k to 1.5k, PR101 1k to 3k
DVT			P49-PWR_VTTP	Add PU23
DVT			P52-PWR_0.75VSP/1.1VSP	Add 0.75VR_EN control signal
DVT			P53-PWR_CPU_CORE	Add PR151, PR191 4.7 ohm, PC118, PC149 680P
DVT			P53-PWR_CPU_CORE	Change PR148, PR188 0 ohm to 2.2 ohm
DVT			P53-PWR_CPU_CORE	Add PC190 0.1U
DVT			P45-PWR_CPU_CORE	Remove PQ40, PQ47
DVT			P52-PWR_0.75VSP/1.1VSP	Change PC101 10U to 4.7U
DVT			P52-PWR_0.75VSP/1.1VSP	Change PC106 SE076104KM8 to SE076104K80
DVT			P45-PWR_CPU_CORE	Change PC151 SE076104KM8 to SE076104K80
DVT				Change PC53, PC54, PC78, PC95, PC181 SF22001M200 to SF000001H00
DVT			P45-PWR_CPU_CORE	Change PR195 1.1k to 1.2k
DVT			P45-PWR_CPU_CORE	Remove PR202 100 ohm, PC150 1200P
DVT			P49-PWR_VTTP	Change PU7 ISL6268 to APW7138
				Remove PC71 0.01U
DVT			P51-PWR_1.5VP	Change PU10 ISL6268 to APW7138
				Remove PC99 0.01U
DVT			P54-PWR_VGA_COREP	Change PU15 ISL6268 to APW7138
				Remove PC164 0.01U
DVT			P51-PWR_1.5VP	Change PL9 SM01000DJ00 to SM010018210
DVT			P53-PWR_CPU_CORE	Change PL11 SM010020720 to SM010018210
DVT			P54-PWR_VGA_COREP	Change PL15 SM01000DJ00 to SM010018210
DVT			P39-PWR_BATTERY CONN / OTP	Change PR33 13.7k to 12.4k
				Change PR37 15.4k to 15.8k
DVT			P47-PWR_CHARGER	Add PR220 4.7 ohm, PC169 680P
				Add PC144 0.1U, PC182 470P
DVT			P45-PWR_CPU_CORE	Add PC113 2200P, PC114 470P, PC138 470P
PVT			P42-PWR_VTTP	Change PL7 0.47U to 1U
PVT			P42-PWR_VTTP	Remove PC66, PC68 10U
PVT			P47-PWR_CHARGER	Change PR70 8.25k to 53.6k, PR72 26.7k to 20k
PVT			P45-PWR_DCIN/DECTOR	Add PC68 680P
PVT			P46-PWR_BATTERY CONN / OTP	Add PD14, PD15
PVT			P42-PWR_VTTP	Remove PR290, PR291, PR292, PR293, PR105, PC228, PC229, PQ55, PQ56
PVT			P47-PWR_CHARGER	Change PR64 PN SD013220B80 to SD014220B80
PVT			P49-PWR_VTTP	Change PR95 PN SD013220B80 to SD014220B80
PVT			P50-PWR_1.05VSP/1.8VSP	Change PR113, PR248 0 ohm to 2.2 ohm
				Add PR114, PR251 4.7 ohm, PC80, PC180 680P
PVT			P45-PWR_CPU_CORE	Change PR148, PR188 PN SD013220B80 to SD014220B80
PVT			P54-PWR_VGA_COREP	Change PR204 PN SD013220B80 to SD014220B80
PVT			P50-PWR_1.05VSP/1.8VSP	Change PR117 8.25k to 4.02k
				Change PR118, PR253 20.5k to 10k
				Change PR252 28.7k to 14k
PREMP			P45-PWR_DCIN/DECTOR	Change PC7 SE041224K80 to SE000005Z80
PREMP			P46-PWR_BATTERY CONN / OTP	Change PR44 13.7k to 12.1k
PREMP			P44-PWR_CPU_CORE	Change PL12, PL14 SH000005680 to SH12036BM00
PREMP			P51-PWR_1.5VP	Change PR131 4.75k to 4.87k
PREMP			P49-PWR_VTTP	Change PR94 1.5k to 39.2k
				Change PR101 3k to 10.5k
PREMP			P50-PWR_1.05VSP/1.8VSP	Remove 1.05V component
MP			P49-PWR_VTTP	Change PR94 39.2k to 6.81k
				PR101 10.5k to 2k
				Reserve for EMI solution (2009/07/23)
				Reserve for EMI solution (2009/07/23)
				Add boot strap resistor (2009/07/23)
				Add snubber (2009/07/23)
				For HW solution(S3 power reduction) (2009/07/23)
				For power test(2009/07/23)
				For HW solution(S3 power reduction) (2009/07/23)
				Add snubber (2009/07/23)
				Add boot strap resistor (2009/07/23)
				Reserve for EMI solution (2009/07/23)
				For design change(2009/07/28)
				For design change(2009/07/28)
				Change to COMPAL PN(2009/08/03)
				Change to COMPAL PN(2009/08/03)
				SF22001M200 is forbids to use (2009/08/03)
				Change Ri for load line (2009/08/03)
				Modify CPU_CORE circuit (2009/08/03)
				For cost down (2009/08/03)
				For APW7138 solution (2009/08/03)
				For cost down (2009/08/03)
				For APW7138 solution (2009/08/03)
				For cost down (2009/08/03)
				For APW7138 solution (2009/08/03)
				Use same PN bead (2009/08/03)
				Use same PN bead (2009/08/03)
				Use same PN bead (2009/08/03)
				Set OTP (2009/08/03)
				Add charger snubber(RF solution) (2009/08/03)
				Add charger snubber(RF solution) (2009/08/03)
				RF solution (2009/08/03)
				Design change (2009/09/04)
				Design change (2009/09/04)
				Set 90W CP (2009/09/04)
				For EMI solution (2009/09/14)
				Reserve for EMI(ESD diode) (2009/09/14)
				Remove VTTP voltage switch circuit(arrandale only) (2009/09/14)
				Use same PN (2009/09/14)
				Use same PN (2009/09/14)
				Add boot trap resistor (2009/09/14)
				Add snubber (2009/09/14)
				Use same PN (2009/09/14)
				Use same PN (2009/09/14)
				Avoid FB trace noise (2009/09/18)
				Change CAP size from 1206 to 0603 (2009/10/09)
				Modify OTP setting (2009/10/09)
				Use 5% tolerance DCR choke (2009/10/09)
				Adjust voltage divided resistor (2009/10/27)
				Adjust VTTPWROK voltage 3.3V to 1.05V (2009/10/27)
				Cost down (2009/11/3)
				Modify resistor for VTTPWROK voltage (2009/11/26)

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